NASA CONTRACTOR REPORT

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NASA CR

AN EXAMINATION OF THE APPLICABILITY OF MICROELECTRONIC CIRCUITS TO THE TELEMETRY AND COMMAND SUBSYSTEMS OF SEVERAL APPLICATIONS SPACECRAFT

Prepared under Contract No. NASw-732 *by*
ARTHUR D. LITTLE, INC.
Cambridge, Mass.
for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • MAY 1965

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I. SUMMARY

A. PURPOSE

The objective of this contract is to study NASA spacecraft electronic systems to identify the circuit functions and subsystems in these which are most susceptible to redesign. The purpose is to incorporate the latest integrated microelectronic circuit techniques, so as to achieve greater reliability and lower power consumption.

B. SCOPE

Task 1 - Study of the telemetry and command systems of the applications satellites, specifically Nimbus and Syncom A. OGO, OAO and IMP were assigned in addition by mutual agreement.

Task 2 - Circuit analysis, taking into consideration proposed designs for incorporating redundancy in the circuits being selected for analysis.

Task 3 - A comparison of microelectronic designs with conventional circuits in terms of weight, size, power, number of interconnections, environmental resistance (including radiation) reliability and cost.

C. APPROACH

Task 1 - The spacecraft telemetry and command systems were studied. Initially, a literature search for published articles on pertinent topics was performed. This was followed by a number of visits to Goddard Space Flight Center for discussion of pertinent details of the electronic systems and subsystems. A number of diagrams and spacecraft documents were analyzed to obtain the required information wherever possible. Elements and subsystems were identified as potentially suitable to the application of microelectronics.

Task 2 - Due to the difficulties encountered in obtaining detailed circuit diagrams and exact values of components in a number of subsystems, the circuit analysis was performed from a system rather than a component approach. A figure-of-merit approach, previously developed, was adapted to the requirements of the spacecraft analysis. The effects of subsystem redundancy were readily included in the figures of merit. Microelectronic circuits were analyzed for their pertinent characteristics and requirements.

Task 3 - Using the principles developed under Task 2, the circuits and subsystems described under Task 1 were analyzed. The characteristics and requirements of both conventional and microelectronic circuit designs were compared. An initial approach used the direct substitution of microelectronic elements, where applicable, for conventional circuits. Furthermore, designs of new elements modified from available ones were suggested. Suitable subsystems were selected which are susceptible to redesign using microelectronic elements.

D. CONCLUSIONS

The microelectronics study has resulted in a number of conclusions, some of which were expected at the inception of the program but which have a quantitative basis as a result of this work. Most of these apply to low-speed, medium-power integrated circuits, since data available on hybrid and thin-film circuits, though encouraging, does not yet provide sufficient information to assess their reliability for near-term use in spacecraft.

- A considerable improvement in reliability of the portions of spacecraft using integrated circuits is now attainable.
- A ten-fold weight and volume reduction in applicable portions of the subsystems is possible.
- One-third to two-thirds of the weight and volume of the telemetry and command subsystems can be eliminated through a redesign with microelectronic circuits.
- Weight reductions, though substantial, represent only a small fraction of total spacecraft weight in spite of the corresponding saving in structure weight.
- Microelectronic integrated circuits do not by themselves reduce the power consumption of spacecraft circuits.
- A larger variety of low-power microelectronic circuits suitable for spacecraft use is still needed, such as switches, multiplexers, dual polarity gates and flip-flops.
- Several common subsystems exist, which can be completely redesigned to permit possible use in several spacecraft.
- Further system redesign is advantageous to implement trade-off possibilities realizable through microelectronics. Thus, one may trade weight reduction for increased power, more integrated circuits for reduced cable and connector wiring, decentralize signal conditioning and switching for increased redundancy and reliability, or reduce power consumption by power commutation with added switching circuits.

II. INTRODUCTION

A. THE BACKGROUND OF MICROELECTRONICS

1. Trend to More Complex Spacecraft

The rise in the functional capability of spacecraft electronics in support of the ever increasing demands of space research has resulted in a continual growth in the corresponding complexity of the electronics circuits within these satellites. This is readily seen from Table 2 - 1 which illustrates the increasing functional complexity and capability of the IMP spacecraft. This was based on the initial designs adapted from Explorer XII, which contained twelve information channels and two hundred transistors, and provided the functional capability of an encoder together with simple switching. The number of information channels has now risen tenfold in the most recent series of IMP satellites, with a corresponding increase in the number of transistors and functional circuit complexity.

This development, however, has been achieved with relatively negligible increases in weight and volume as well as in the power drawn from the satellite electronics. It has, in fact, been based almost entirely on the improved capabilities for performance of modern electronic components and on advances in circuit assembly techniques. A further increase in the use of microelectronic components can provide the means for achieving additional functional capability without further increases in size, weight or power.

This greater functional capability as well as the increasing complexity is a trend that has occurred in electronics during the last decade and is expected to continue. Thus, the needs for more compact electronic systems of a higher degree of reliability are not unique to the spacecraft field. Rather, the developments of computers and military equipment and many other types of electronic systems are developing in these same directions although they require a somewhat different level of complexity and of reliability than the space applications. Thus, the field of space electronics can frequently utilize techniques which were developed for other military equipment or commercial computers to achieve a better electronic system.

Figure 2 - 1 illustrates the number of circuit functions per equipment of small and large computers as well as airborne and ground based military equipment for comparison with those described in IMP. Although, in general, the increase in functional capability has not grown as rapidly as in the spacecraft example previously illustrated in Table 2 - 1, nevertheless the same trend appears almost universally.

TABLE 2 - 1

FUNCTIONAL COMPLEXITY OF IMP SPACECRAFT

ELECTRONIC SYSTEM

Spacecraft	Information Channels	Number of Transistors	Functions Added
Explorer 12	20	200	Encoder
Ariel 1	90	600	Commutator
IMP 1, 2, 3	175	1,200	Accumulator
IMP 4, 5	256	$>$ 2,000	Digital Data Processor

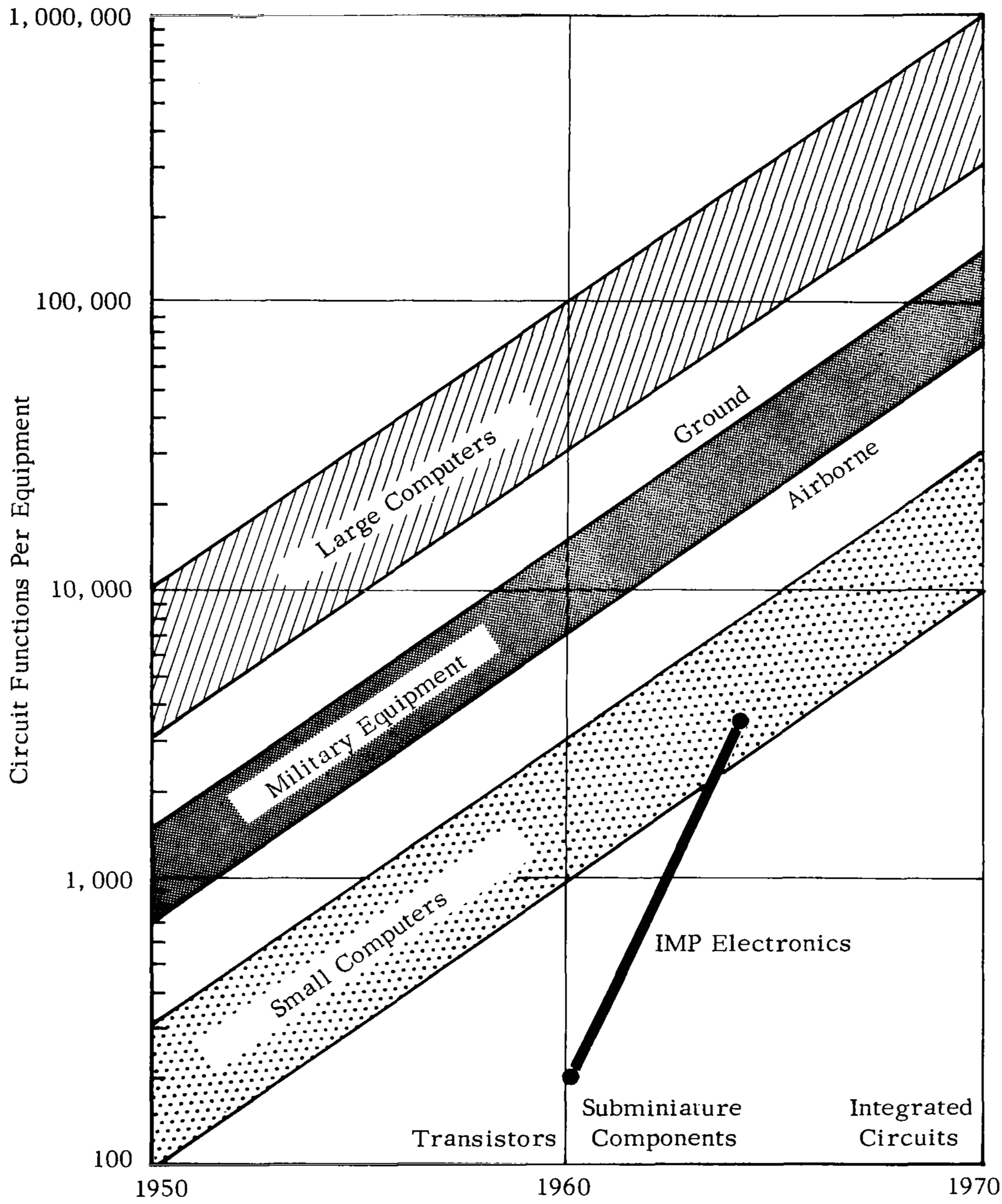


FIGURE 2.1 RISING COMPLEXITY OF ELECTRONIC EQUIPMENT

As complexity increases, the likelihood of breakdown also becomes greater; thus, at the same time as manufacturers have been trying to lower the cost of active and passive circuit elements, they have also been under very great pressure to reduce component breakdown. Only thus can one improve equipment reliability so that the present-day complex equipment is even more reliable than its simpler predecessors.

The corresponding trend towards miniaturization, that is towards smaller sizes of component parts, is apparent from Figure 2 - 2. The size of component parts has been steadily reduced during the last decade. This permits the increasingly complex equipment to occupy about the same volume as before. Weight has followed suit. The newest aerospace computers, for example, have about the same or even less weight than those designed a few years ago. This great incentive for microminiaturization and the use of microelectronics in aerospace electronics is caused by the great needs for more functional capability with less weight; without substantial miniaturization such complex electronic equipment would literally never get off the ground. It is achievable because the material content and the space occupied by the working region of most low power electronic components is extremely small. The active area within a transistor measures only a few thousandths of an inch in each dimension and in many cases resistor and capacitor functions can be accomplished within a volume that is only slightly larger. Thus, a great deal of the miniaturization of components is really only squeezing out air and waste space previously occupied by empty volume and by connecting pieces. This is also illustrated by the figures on OSO and AOSO designs in Table 2 - 2. Figure 2 - 2 also compares the degree of miniaturization possible from cordwood construction as well as from thin-film, hybrid circuits with microcomponents and finally from semiconductor integrated circuits. Even the latter, placed on a small printed circuit board, still occupy a volume ten times larger than that of the actual "solid circuit" package which could be packed into a density exceeding ten million parts per cubic foot if we only knew how to interconnect them without requiring a much greater volume.

Such tight packing density would require substantially lower power dissipation than is currently available from such units, as otherwise we would have serious problems of internal heat dissipation. In fact, at the moment the small size and low failure rate of semiconductor integrated circuits has outstripped our ability to utilize these most effectively in electronic equipment. The next few years will see the development of a still greater variety of such monolithic and hybrid circuits to extend their area of usefulness to a wider range of electrical circuits applicable to spacecraft as well as other areas of electronics.

2. The Classes of Microminiature and Microelectronic Components

Figure 2 - 3 illustrates the trend with time toward the use of the various microelectronic approaches for miniature components and

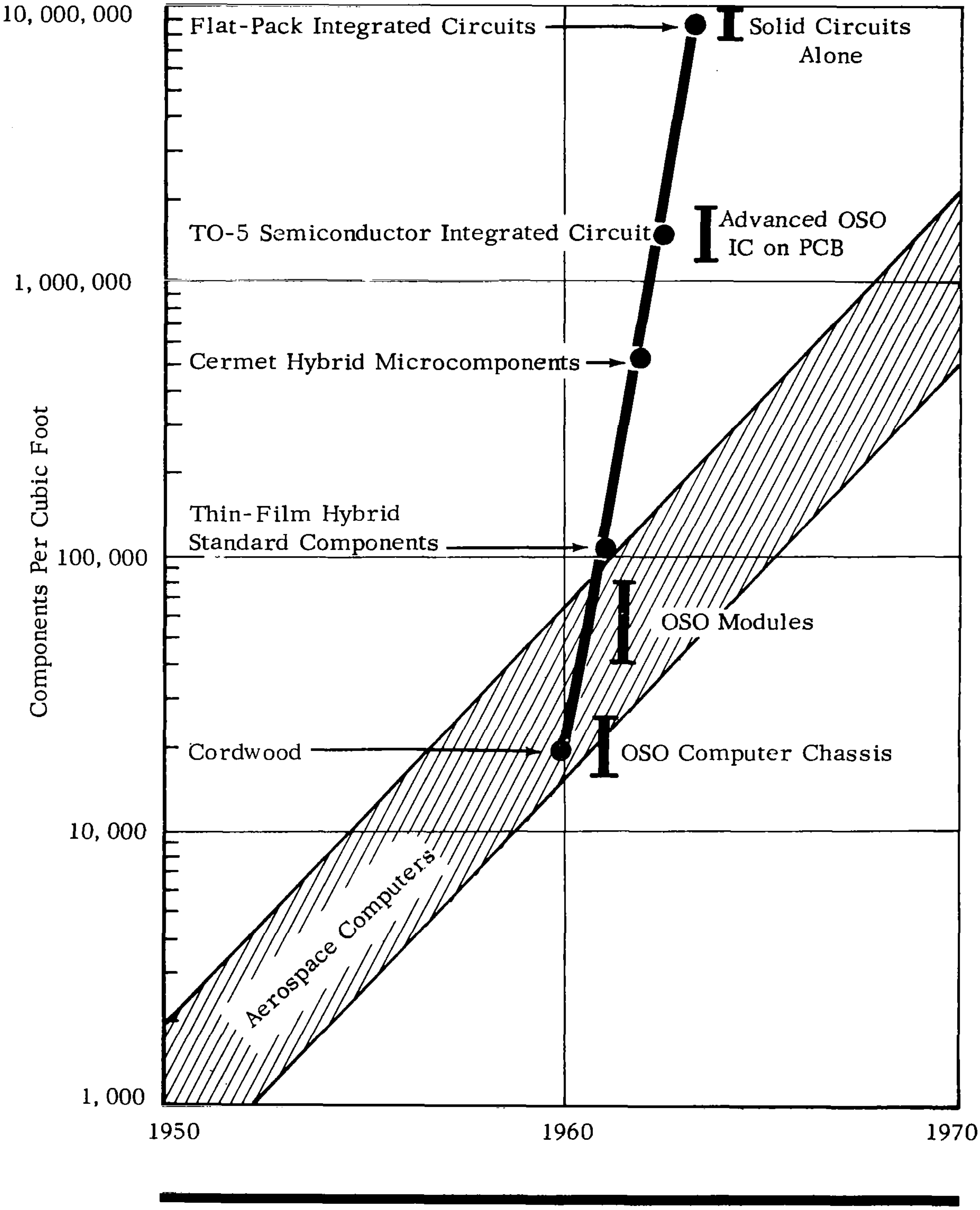


FIGURE 2.2 MINIATURIZATION OF OSO

TABLE 2 - 2

PACKING DENSITY OF OSO SPACECRAFT ELECTRONICS

	Parts Per Cubic Foot	Avg. No. of Components	Volume (cu. in.)
Computer Chassis	13 - 25,000	3,000 - 6,000	375
Cordwood Module	40 - 80,000	10 - 20	0.44
Integrated Circuits* on Circuit Boards	1,200,000	160,000	21.6
Integrated Circuit* Package	10,000,000	30	0.003

*Note - Using thirty components per integrated circuit.

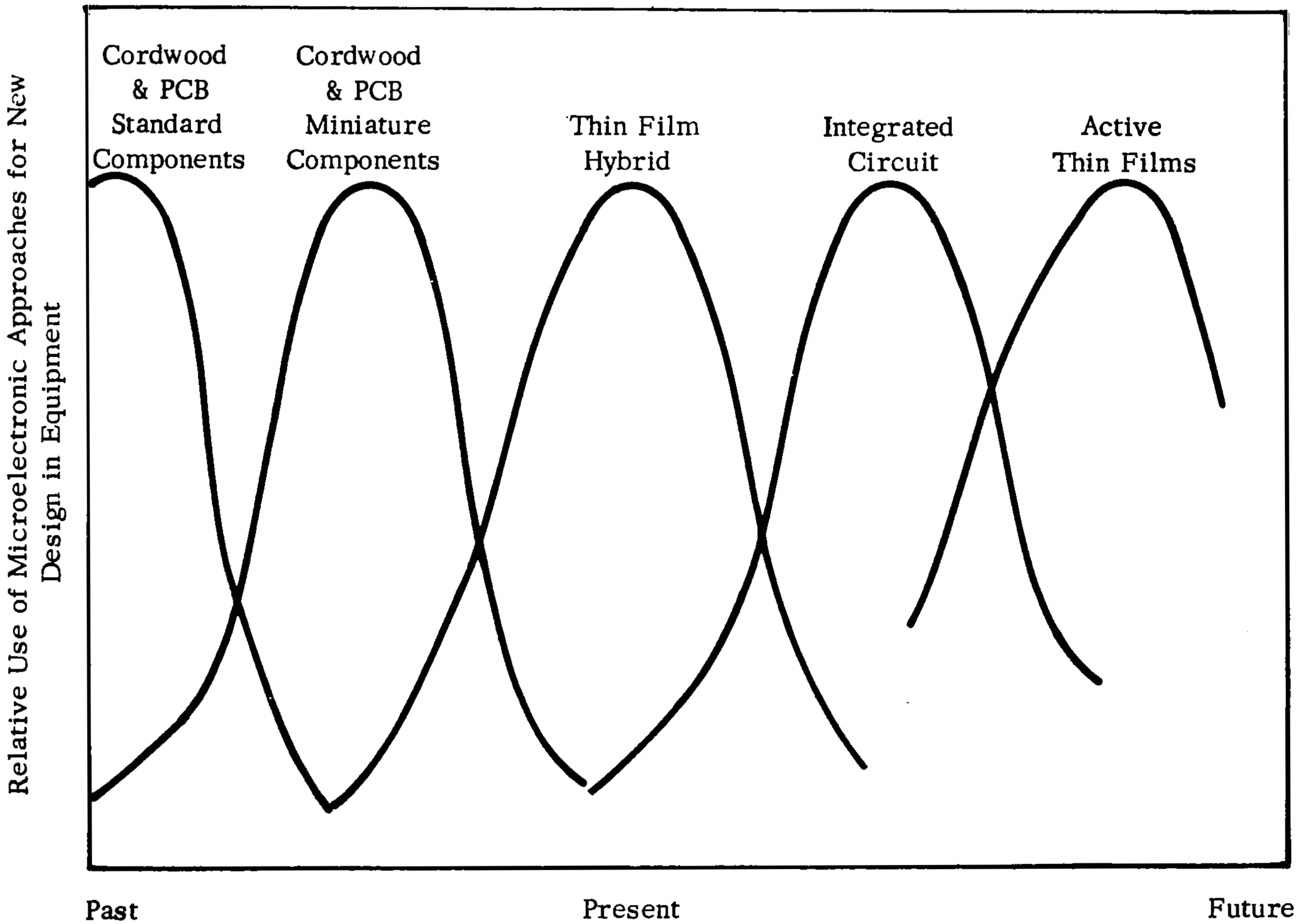


FIGURE 2.3 NEW DESIGN USAGE OF MICROELECTRONICS

integrated circuits. Initially, the miniature electronic equipment for spacecraft was put together using small but standard components on printed circuit boards. This very rapidly became displaced by the cordwood technique of assembly which had been developed for other aerospace equipments. By now, the cordwood technique as well as miniaturized printed circuit boards are in use in most of the satellite electronic circuits, using the best and most reliable but smallest available present-day miniature components. Some circuits are also using thin-film hybrids which use discrete transistors and diodes in conjunction with printed resistors and capacitors fired onto a ceramic substrate. This "cermet" technique will see considerable near-term use both in analog and in digital circuits. In many applications, however, silicon integrated circuits are most suitable and will be used more and more.

It is readily seen that, as current practice develops, each of the approaches is favored most for a particular period of time, and yet as the newer components of even more compact size are developed, they tend to be incorporated in the next wave of new electronic spacecraft equipment. This is a direct outgrowth of the fact that at one time the particular needs for smaller size in a given spacecraft were not too severe, and it is only after that particular generation of equipment has been built and tested that a further reduction in size using the next more advanced type of microelectronic components becomes useful.

This is shown by the experience with the Explorer and IMP satellites, illustrated in Table 2 - 1. Explorer XIV was constructed with printed circuit boards and soldered components, whereas the latest IMP series contains all welded connections, cordwood and printed circuit assembly techniques, and includes a few integrated circuits. The further development of assembly and construction techniques is expected to result in a much greater application of integrated and thin-film hybrid type circuits.

3. Methods and Trends in Interconnections

It is appropriate in a microelectronic study to look also at the methods of component and system interconnections since many of the requirements of this are completely pertinent to the engineering decisions which must be reached in selecting the choice of a microelectronic component. The satellite and ground stations together can be considered as a complex telemetering system whose function is to transmit the measurements from numerous sensors to the ground and, of course, communicate confirmation and selection signals back to the satellite. Thus, the complex satellite system is made up of several so-called normal systems connected by antenna and radio links, one of these normal systems being the ground station and another one the satellite electronic system itself. Within the satellite system a number of subsystems are constructed on separate equipment chassis and connected to each other by cables and plugs. Each such chassis contains numerous modules or printed circuit cards which are connected to each other into the chassis with wires, solders or welds and further cables. This is outlined in Figure 2 - 4.

The various components on each printed circuit card are interconnected by the printed circuit itself, fastened with soldered or welded connections. In this example, a complete satellite electronic system is, therefore, composed of four levels: the total system level, the subsystem level, the module level and the component level. Sometimes an extra level between the subsystem and the card exists, if several small chassis are required to make one subsystem. In assembling a highly reliable and maintainable electronics system, one tests the parts at each level as well as possible, and then requires sufficient interchangeability among equivalent pieces of subsystems or modules that in case of failure the piece at that level of circuitry may be replaced by a working one. The ultimate reliability of the total system is then computed from the measured and thoroughly tested reliability of the high-use components and guesses as to other parts of the system. In a conventional system the reliability is calculated by an extrapolation to the fourth level of the system from the component figures.

In the case where the microelectronic circuits such as integrated or hybrid circuits are used to replace the original modular card, a reduction by 1 in the number of levels of such equipment and interconnections is immediately achieved, since such integrated or functional blocks can be fully tested to the same types of environmental specifications to which individual components were previously tested. The results of reliability tests on integrated circuits are now only extrapolated through three levels, one less than in the former case.

Aside from any numerical differences between the reliability results from discrete and integrated components, a very important but intangible gain is the elimination of the discrete component level through the use of microelectronic circuits. Ultimately, upon the achievement of increased reliability and much smaller weight and size of such microelectronic systems one will build even more complex ones, then an additional "complex system" level will be added.

4. Methods of Assessing and Characterizing Microelectronic Circuits

A number of approaches exist to microelectronics. Four of the most common ones are the discrete miniature components, the thin-film hybrid networks, the semiconductor integrated circuits and the thin-film active devices, as shown in Figure 2 - 5. The discrete miniature components have been in existence for a considerable period of time; and although new types are constantly being developed with better and

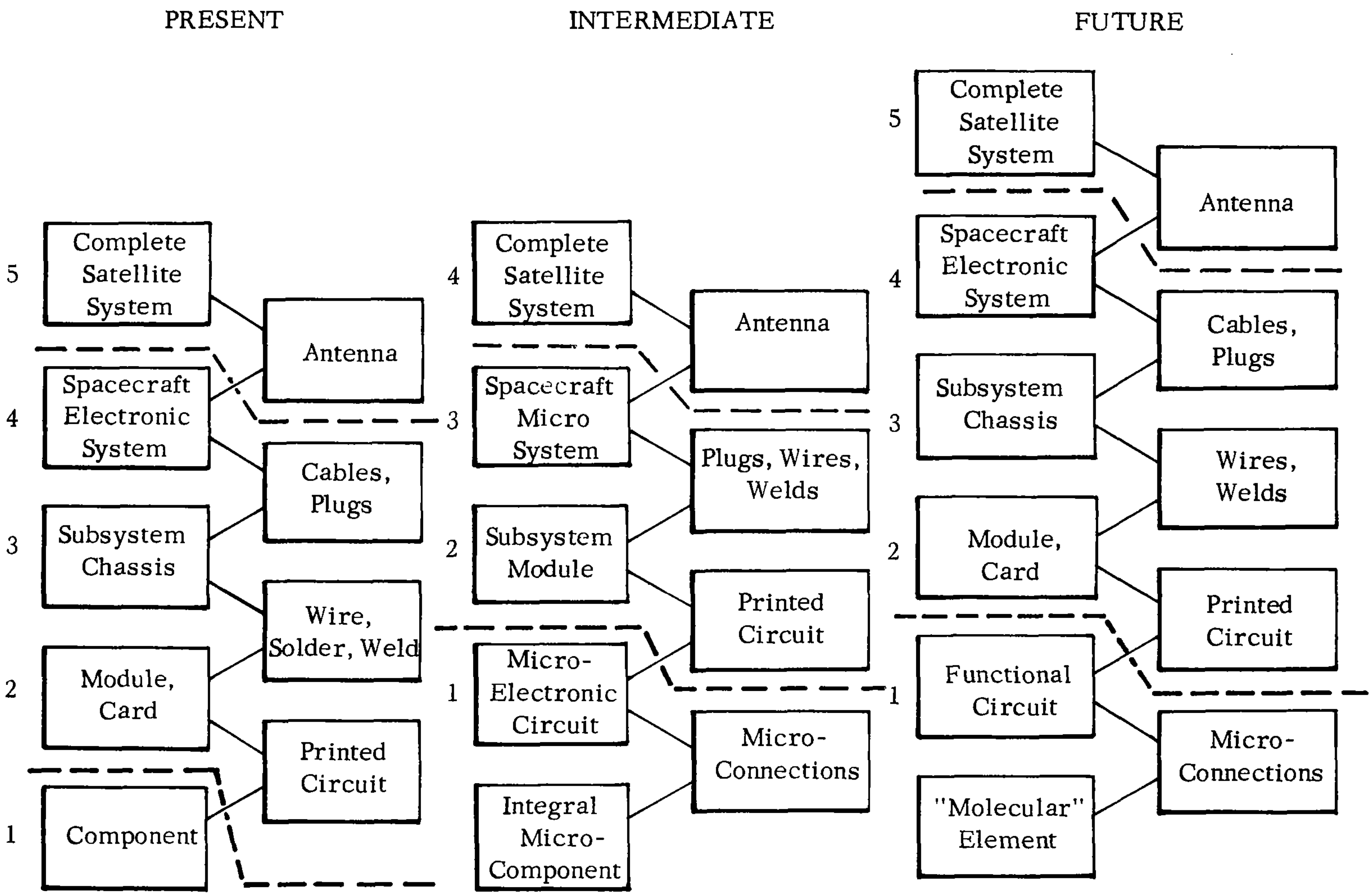


FIGURE 2.4 LEVELS OF COMPONENT AND SYSTEM INTERCONNECTIONS

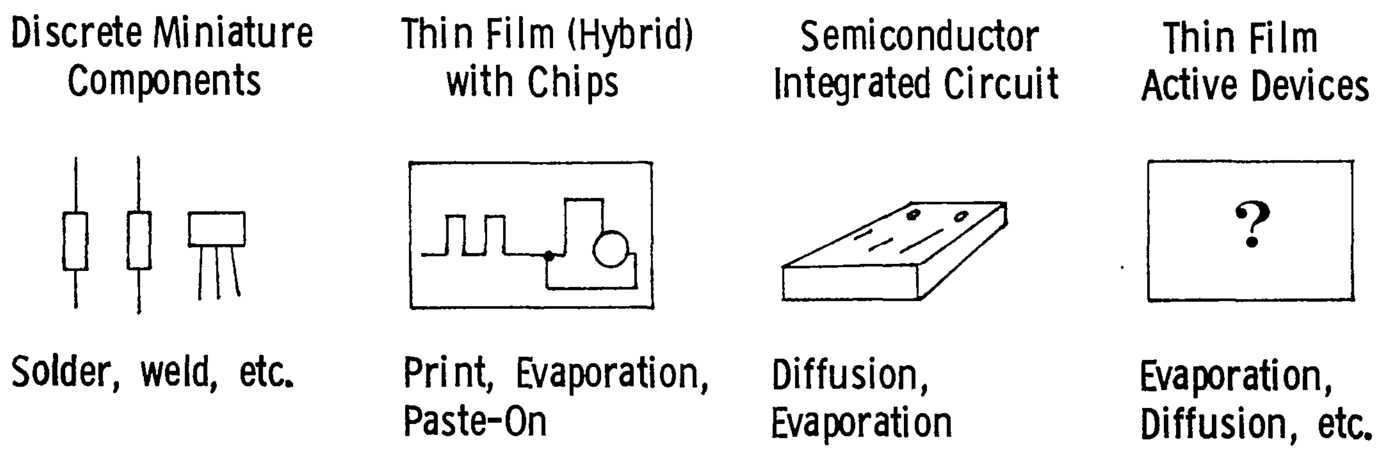


FIGURE 2-5 APPROACHES TO MICROELECTRONICS

better performance, they are not discussed in great detail in this study. Thin-film hybrid circuits have seen increasing use, particularly in those areas of electronics where a very high degree of stability of passive components is required, or where performance at very high frequencies is necessary. These are made variously on a single substrate by evaporation, by silk screen printing of cermet components, as well as by other methods better known from discrete miniature components, as shown in Figure 2 - 6. Generally the active devices, such as transistors, have been soldered or alloyed onto the ceramic substrate holding the thin-film or printed passive network.

The semiconductor integrated circuit has now been available for several years. This is based entirely on silicon planar and epitaxial technology and both active and passive components are created by diffusion, evaporation, and epitaxy. These are extremely well suited to digital and in some cases to the analog circuits of satellite electronics. However, frequently much lower powers would be desirable than are currently available from commercial and military type integrated circuits. Finally, the thin-film active devices are being aggressively developed at the moment but have not yet reached the state of development which will allow regularly produced components to be incorporated into the present and near future designs of spacecraft.

As well as these four major classes of integral circuits or complex components a number of hybrid combinations exist, Figure 2 - 7. For example, the thin-film hybrid circuit uses a passive film network on a substrate with those discrete components added externally which could not be so deposited. An alternate method is to use a semiconductor wafer and apply those thin-film resistors and capacitors over its surface which are more appropriately made in this fashion rather than being formed within the semiconductor. Finally, when thin-film active devices become available, there will no doubt be hybrid types using silicon technology as well as thin-film tunneling and field effect techniques to provide the best combination of characteristics on one chip.

Besides the printing method it is convenient to remember the other methods of assembling or making a variety of integrated and other microelectronic circuits such as by vacuum evaporation, cathode sputtering, semiconductor techniques, hybrid technology, thermal decomposition and epitaxial or other vapor plating. These are illustrated in Figure 2 - 8.

5. Characteristics

In order to survey the uses and applications of the major microelectronic approaches to particular portions of a spacecraft electronic system, one must first consider the capabilities of these in general terms. The expected reliability per function, resistance

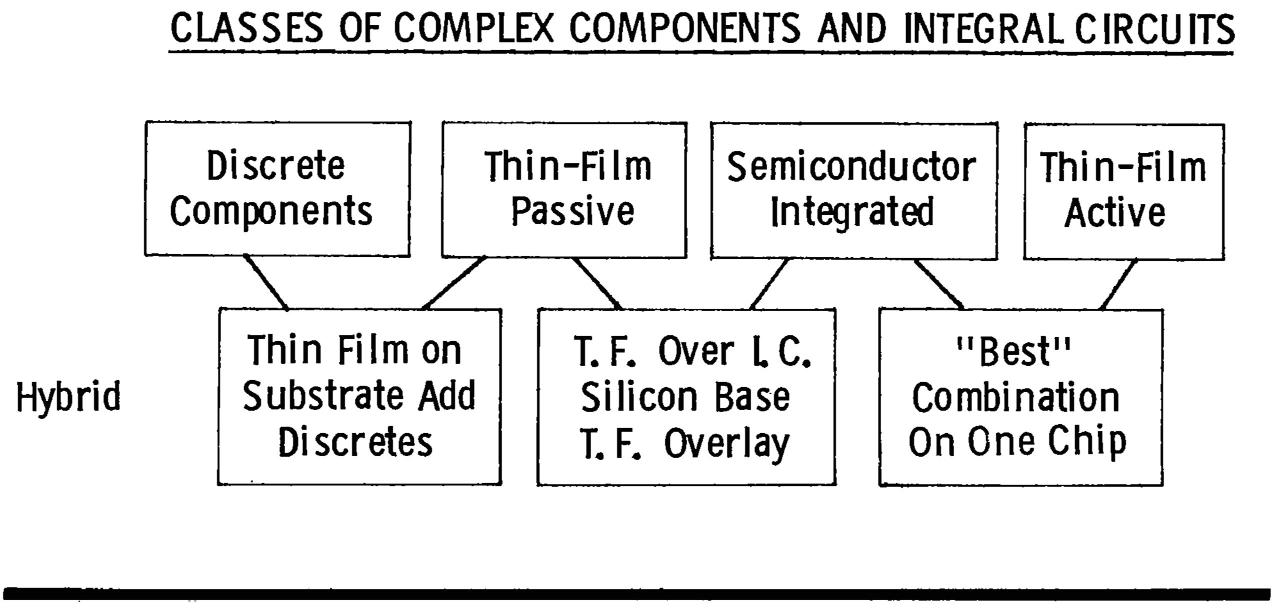
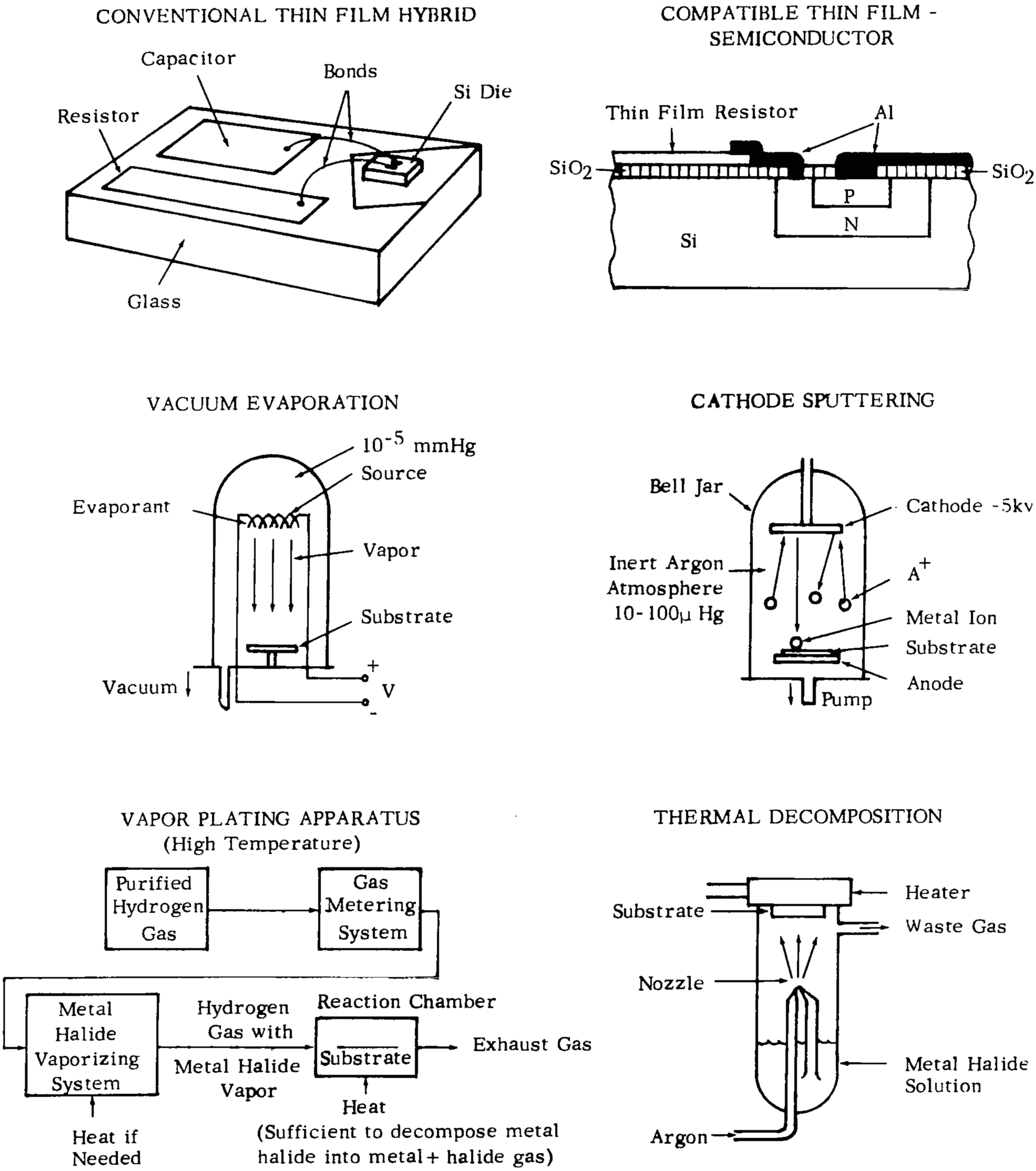


FIGURE 2-6 CLASSES OF COMPLEX COMPONENTS AND INTEGRAL CIRCUITS



Sources: Courtesy Motorola - Integrated Circuits Course

FIGURE 2.7 FABRICATION TECHNIQUES USED FOR SEMICONDUCTORS AND INTEGRATED CIRCUITS

range, range of capacitances and inductances, power dissipation as well as speed or repetition rate are compared for currently available discrete circuits, thin-film hybrids, semiconductor integrated circuits, and the expectations for thin-film integrated circuits using thin-film active elements. Table 2 - 3 shows this comparison.

TABLE 2 - 3

CAPABILITIES OF MICROELECTRONIC CIRCUITS

		Miniature* Discrete Circuits	Thin-Film Hybrid	Semicon. Integrated	Thin Film Integrated**
Reliability per Function (mean time to failure, hr)	Present	10^6	10^6	10^6	--
	Future	10^7	10^7	10^8	--
Price per Function (mil Specs)	Present	$20	$20-$40	$10-$80	--
	Future	$10	$ 5-$10	$ 1-$ 2	--
Resistance Range (ohms)	Present	$1-10^6$	10^2-10^6	10^2-10^4	--
	Future	$1-10^6$	$10-10^7$	$10-10^5$	$10-10^6$
Capacitance, max. (farads)	Present	10^{-6}	10^{-8}	10^{-8}	--
	Future	10^{-5}	10^{-7}	10^{-8}	10^{-7}
Inductance, max. (Henries)	Present	10^{-2}	10^{-5}	Negli.	--
	Future	10^{-2}	10^{-4}	Negli.	Negli.
Speed (megacycles) Pulse repetition, f	Present	20	20	10-50	--
Gain - bandwidth, ft	Present	100-400	100-400	200	--
	Future	5,000	5,000	1,000	1,000
Power, upper limit	Present	Watts	Watts	Watts	--
	Future	Watts	Watts	Watts	Watts
Ability to breadboard	Present	Exc.	Good	Poor	--
	Future	Exc.	Exc.	Good	Good
Design to produce time	Present	Days	Weeks	Months	--
	Future	Days	Days	Weeks	Weeks
Design and change flexibility	Present	Exc.	Med.	Poor	--
	Future	Exc.	Good	Med.	Med.
Size (parts/cu. ft.)	Present	10^5	10^7	10^8	--
	Future	10^5	10^7	10^9	10^9

---

*For meaningful comparisons, these figures are for semiconductor circuits using miniaturized discrete components.

**Since thin-film active elements are still in the laboratory, values are listed only for those future capabilities that can be roughly estimated.

B. DEVELOPMENT OF SATELLITE TELEMETERING

This is illustrated in Table 2 - 4. The earliest space satellites contained relatively few electronic circuits, whose primary function was to transmit the telemetering data on relatively few experiments. Very elementary forms of multiplexing were used so that the electronics system was really the transmitter serving a collection of experiments.

As the number of scientific experiments aboard the larger satellites grew, certain additional electronic features were added. The data was multiplexed to accommodate the larger number of channels in a central commutating subsystem and a few experiments were turned on and off either on command from the ground or from clock signals. Thus, these types of satellites are characterized by having rudimentary control features as well as the data multiplexing. The systems at this stage of development are represented by the telemetering and command features of the earlier Explorer and IMP type satellites, Table 2 - 1. As the electrical load on the satellite power system grows with the larger number of experiments and the greater amount of data to be transmitted, central data conversion was used in order to eliminate the duplication of signal conditioning, A/D conversion and format generation within the electronics subsystem of each separate experiment. This is shown by many of the present generation of satellites, which have an integrated data conversion system as well as fairly elaborate command and control features associated with the telemetering transmitters and command receivers. There may be several data conversion and switching subsystems in order to provide a certain degree of redundancy in case one section should fail but the attempt has been to provide as much of the electronic data processing and switching in the central electronics system as possible. It is at this stage that we are now, at which microelectronics is being considered for simplifying and improving the performance of the telemetering and control subsystems of the applications satellites.

Progress in this direction is occurring in two phases: the present phase focusses attention on the microelectronic elements with the goal of a reduction of power, weight and size, and a substantial improvement in the failure rate. Also new types of microelectronic elements will be developed during this phase which will be directly applicable to the more specialized needs of certain spacecraft circuits rather than being adapted from the catalog of presently available types. Upon accomplishing these goals and applying available and newly developed microelectronic elements wherever possible within the satellite, a second phase will occur. Trade-offs with the power and mechanical features, with the electronics in the experimental portions of the satellite, and other re-optimization will result in a further improvement of reliability and of other features of the satellite. This will

TABLE 2 - 4

DEVELOPMENT OF SATELLITE TELEMETERING

1. Collection of experiments, elementary multiplexing

2. Central data multiplexing and control, experiment command features

3. Central data conversion, integrated system eliminates duplication

4. Microelectronics: Phase I - elements, existing and new

   Reduction of failure, power, weight, size

5. Microelectronics: Phase II - system optimization

   Trade-offs with wiring, power, mechanical, experiments

   Decentralized system, duplication and redundancy bring about a decentralization of the electronic system, since the weight and power drain of many microelectronic elements are sufficiently small that advantages are gained by duplication of functions and the use of greater redundancy. This second phase shows a trend towards the decentralization of the electronic systems.

C. A METHOD OF CHARACTERIZING MICROELECTRONIC PARTS

A method of characterizing microelectronic components and functional electronic blocks is available. This is suitable for comparing a number of approaches to a given function and developing figures-of-merit which can be used for a quantitative comparison and ranking of these approaches. The method is based in part on a paper entitled "Performance Figures-of-Merit for Integrated Circuits" by Dr. H. Gunther Rudenberg, prepared last year for presentation at NEREM, Boston, Massachusetts, in November 1963.

In most applications to space electronics, the cost of using a circuit is not based on its price and related dollar expenses. Rather, other non-circuit portions of the total system have such a high monetary cost that other than monetary considerations apply to the electronics. Whatever factors are severely limiting -- such as failure rate, weight, volume, power supply or the total allowable thermal dissipation -- will determine the "expense" factor of using the circuit. In the field of space electronics, the weight is the paramount "expense" factor; and wherever satellite power supplies limit total available power, the current and power drawn per circuit determines its "expense" factor. Sometimes the space that can be allocated to an electronic system is severely limited, and then the volume, or possibly the area, of circuitry determines its "expense". Finally, for extreme microminiaturization, the thermal dissipation may be an applicable factor.

A variety of performance parameters can be selected to define a useful figure of merit, but very few will suffice for most engineering applications. One of these, important in analog or linear amplifiers, is the total gain of a circuit stage. For low frequency audio and radio (linear) circuits, one uses primarily the gain as a performance measure. Here the limiting bandwidth of solid state device circuits is never exceeded and the circuit impedances determine the maximum practical gain available from each specific device. A distinction has to be made also whether resistance coupled or transformer coupled interstage circuits are used, as each of these application areas has different limits on practical performance. By using the logarithmic value of gain, we obtain the gain-performance figure of merit suitable for a consideration of cascaded stages. In the area of high-frequency amplifiers, however, the pertinent parameter is naturally the gain-bandwidth product. Here again, the logarithm of this number is used.

Considering the areas of digital circuit applications, such as switching and digital data processing, it is apparent that two important areas of application present themselves. Most real-time computing applications are not speed limited, since the rate of data input is already fixed. Here naturally, the number of decisions per circuit or system is used to measure performance. This applies to many satellite electronic circuits. Other computing systems become more efficient the faster they operate, so that in this area the decision rate must be used, particularly if serial logic is utilized.

Other specialized areas frequently require special performance parameters. For output circuits, either digital or analog, the power, charge or current available determine their performance, and in cases where high frequencies are involved the power-frequency product, or current per unit time, are important. Table 2 - 5 presents the most useful parameters that could be compared.

Less tangible but also very important characteristics like low noise, long term stability or reliability will also have to be considered, Table 2 - 6.

These are less amenable to direct measurement and comparison, and are more difficult to factor into suitable quantitative figures of merit. Mean-time-to-failure or life may be a factor suitable in the case of simple replaceable solid state systems. In redundant systems with complex interconnections, it is possible that the logarithm of the life of each subsystem would provide a more useful number for the applicable performance parameter.

The figure of merit for each case is the ratio of an applicable performance parameter to the most useful "expense" factor. Thus, a gain figure of merit in decibels gain per dollar of circuit cost can be used to compare a linear integrated amplifier with its discrete prototype in respect to its relative usefulness when price is important. For the low-speed logic section of a space satellite, a useful figure of merit would be the number of bits per unit weight. In each case, the quantitative comparison of the figure of merit of various competing circuits will aid in the selection of the most "economical" one for the required performance. Table 2 - 7 illustrates several of the more useful permutations of such factors for an analog type integrated circuit.

This approach provides the mechanism for a simple method of comparing a variety of microelectronic circuits with each other by listing the useful performance parameters and "expense" factors, and using applicable ratios as figures-of-merit for selection and design.

In the work under this contract, a more elementary approach was used. Here, those "expense" factors of the existing discrete and the suggested microelectronic circuits are listed which provide equivalent performance. The performance is considered equivalent if one circuit can be directly substituted for another, and such a direct comparison avoids a quantitative determination of the performance factors of either the circuits or the subsystem considered.

TABLE 2 - 5

PERFORMANCE PARAMETERS CHARACTERIZING CIRCUIT

Applications	Performance Parameter	Units
Linear		
DC or Audio	Gain	db
High Frequency	Gain-Bandwidth	log (G.B.)
Digital		
Low Speed	Digits or Bits	N
High Speed	Bit-Rate	N/sec
Parallel	Fan-Out	K; log K
Output		
Power	Output Power	Watts
High Frequency	Power-Frequency	Watts/second
High Voltage	Charge	Coulombs
Magnetic Drive	Current-Frequency	Amps/second

TABLE 2 - 6

OTHER CONSIDERATIONS

	Performance	
Reliability:	Mean-Time-To-Failure, Stability, Signal-To-Noise, Interchangeability Cross-Talk.
Characteristics:	Impedance, Fan-Out, Tolerance and Range, Logic Capability, Frequency.
	"Expense"
General:	Mask Cost, Reliability Cost, Leads and Package, Design and Assembly Time.
User Constraints:	Repairability, Standardization, Spare Parts Logistics, Popularity.

TABLE 2 - 7

LISTINGS FOR FIGURES OF MERIT

Performance Value		Price $ U	Weight grams V	Volume cm^3 X	Power mW Y
Gain (db)	A	A/U	A/V	A/X	A/Y
Gain-Bandwidth	B	B/U	B/V	B/X	B/Y
Output (mW)	C	C/U	C/V	C/X	C/Y
Power-Frequency	D	D/U	D/V	D/X	D/Y

The "expense" factors, such as weight, power drain, volume, number of connections and components, reliability factors and so on are then listed, Table 2 - 8, and added after suitable weighting. The summation of these factors then provides a measure of the corresponding weight, volume, power drain and reliability of the subsystem for the original or the microelectronic version of the circuit, as required under Task 3.

TABLE 2 - 8

"EXPENSE" FACTORS

*Failure rate	Cost
*Weight	*Weight with chassis
*Power drain	Current drain
Volume	Volume with chassis
*Number of components	*Number of connections

*These are primarily considered in this study.

III. TASK 1 - SPACECRAFT STUDY

The work accomplished under this task includes an analysis of the spacecraft electronic systems, and the identification of those subsystems and elements which are common to several of the satellites. The electronic systems of the following spacecraft are discussed in Table 3 - 1.

Primary emphasis has been placed upon the telemetry and control subsystems, which include switching, signal conditioning, data processing and communication functions.

A. IMP SPACECRAFT ELECTRONICS

The Interplanetary Monitoring Probe (IMP) or platform (also termed program) has been developed out of the EXPLORER family of exploratory satellites. Their purpose is to carry out a moderate number of space measurements, such as magnetic fields, ionization levels and types, particle counts and others suitable for the detection of radiation hazards and solar flares. Successive units may carry quite different experiments, but the central electronics core was initially thought to be the same and highly standardized.

Actually, the electronics system has been developed and refined during successive re-designs, so that it has also been adapted to each new demand. Most of the information pertinent to this study was derived from the rather complete documentation on the circuits for the S-74 model of IMP and for the earlier EXPLORER XIV (S-3A). These weigh 135 lbs. and have a 24 watt power supply. EXPLORER had a circular earth orbit; the IMP series uses a larger booster to launch the probe into a highly eccentric orbit so as to traverse 180,000 miles into deep space in an earth-bound orbit.

The small satellite is designed to carry eight experiments into the highly eccentric orbit. The purpose of these experiments is to measure the cislunar environment. The central portion of the electronics in IMP is for data processing and telemetry and is shown in the attached block diagram, Figure 3 - 1.

The telemetry format is a sequence of 256 channels arranged in sixteen frames of sixteen channels each. The channel rate is 3-1/8 channels per second, and the complete sequence lasts 81.92 seconds. The format is sub-commutated; three normal sequences as described above are followed by a "Rubidium" sequence, 81.92 seconds reserved for the output of the Rubidium magnetometer alone.

TABLE 3 - 1

SPACECRAFT STUDIED

IMP	OGO
Nimbus	OAO
Syncom A	AOSO

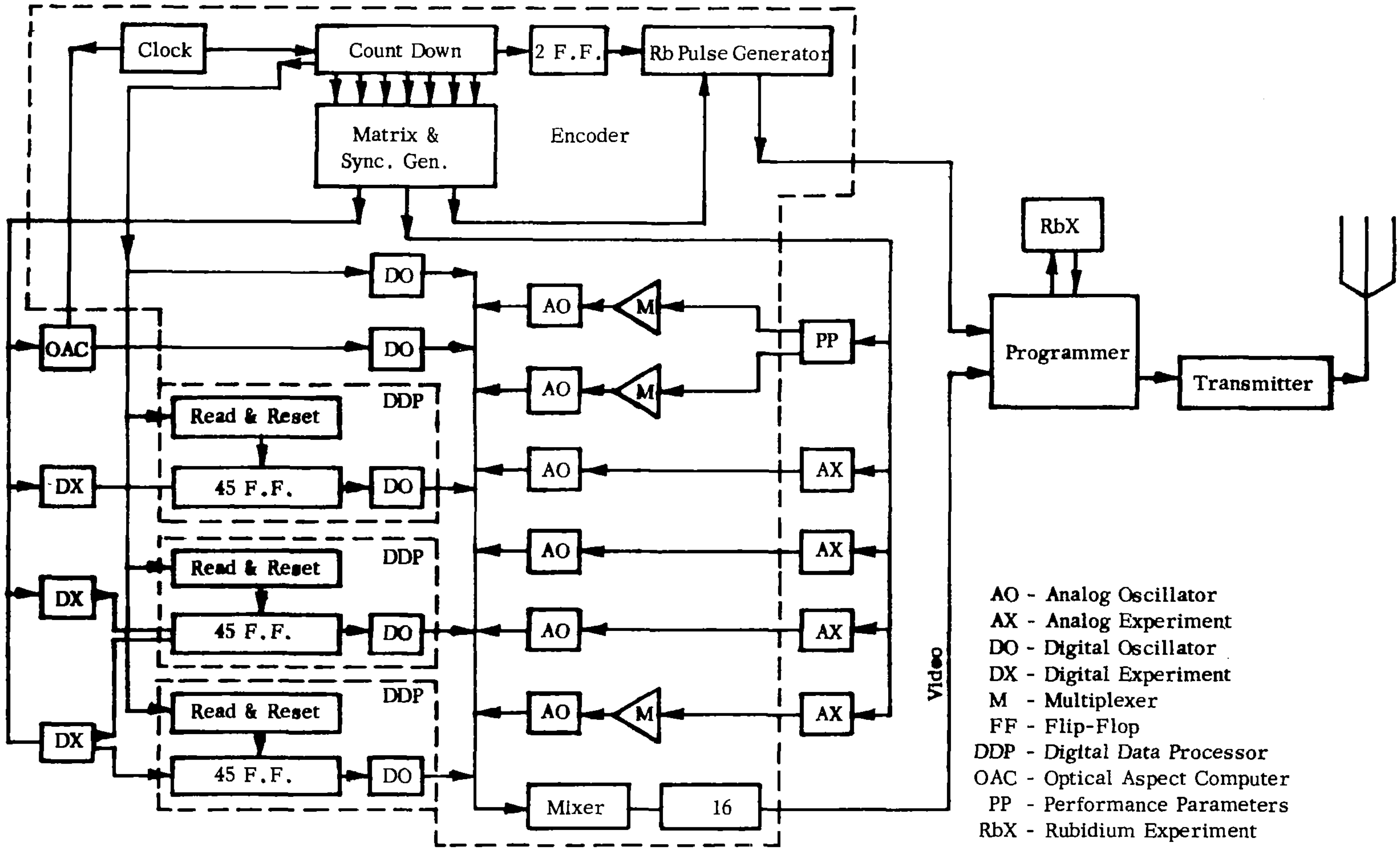


FIGURE 3.1 IMP - BASIC ELECTRONICS BLOCK DIAGRAM

Information is encoded by pulse frequency modulation (PFM). Analog data is converted from voltages in the range 0 to +5 volts DC to a frequency in the range 15 to 5 KC by "analog" oscillators. Digital data is converted three bits at a time to one of eight frequencies in the range 5 to 15 KC by "digital" oscillators. Before transmission these frequencies are lowered by a factor of sixteen by counting down. This allows the use of the PFM system developed for the EXPLORER system, and the sixteenfold countdown provides the lower data transmission rate required for the larger transmission distance of the IMP system. All the oscillators are similar, being linearly or digitally steered in frequency by the input data signals. Note that the electronics are greatly simplified by this method of encoding. Analog and digital data can be treated identically after the data oscillators, and no analog to digital or digital to analog conversions are required within the satellites.

The telemetry subsystem consists of three digital data processors (DDP) and an encoder. A typical digital data processor contains forty-five flip-flops in blocks of three arranged in a number of accumulators, a logic network for readout and reset functions and a digital oscillator. The encoder contains the clock, the countdown flip-flops, the synchronization generating matrix, the analog oscillators, some digital oscillators and a few other circuits. The telemetry subsystem contains 1,129 transistors and 11 tunnel diodes, a total of 1,140 active devices. The electrical power required is shown in Table 3 - 2 and is supplied by the encoder converter. The power supplied to this at a converter efficiency of 50% is .78 watts.

The power requirements and weights of the major units in IMP are summarized in Table 3 - 3. The first column lists the power used by each unit, including individual converter losses, while the second column lists the load placed on the primary power system and includes the losses in the prime converter which is 68% efficient. The actual weights of the units are listed in column 3. When one distributes the weight of the structure and miscellaneous items over the electronic portions of the satellite on a weight proportional basis, a weight correction factor of 1.387 is obtained. These results are illustrated in column 4. The weight "cost" of power is 56.5 lbs./37.0 watts or 1.527 lbs./watt (693 g/watt).

TABLE 3 - 2

POWER USED IN IMP TELEMETRY SUBSYSTEM

+6.7 v @ 25 ma	=	167.5 mw
+1.9 v @ 12 ma	=	22.8 mw
-4.2 v @ 40 ma	=	168.0 mw
-2.7 v @ 14 ma	=	37.8 mw
		396 mw

TABLE 3 - 3

IMP - WEIGHT AND POWER

Subsystem	Power, Watts		Weight - Lbs.	
	Average Used	Average Required	Net	Structure Redistributed
Experiments including Optical Aspect and Performance Parameters	10.53	15.49	38.1	52.9
Transmitter and Range Rate	12.54	18.44	7.0	9.7
Telemetry Subsystem	.78	1.15	5.8	8.0
Programmer and Misc. Power	1.31	1.92	6.0	8.3
Total Power Supply (Batteries, Solar Cells, Converters and Regulators	--	--	40.7	56.5
Structure and Misc. Weight	--	--	37.8	--
TOTALS	25.16	37.0	135.4	135.4

B. SYNCOM

The Syncom satellite is an active repeater serving to relay communications between distant points over part of the earth's surface. It will hover nearly stationary at a height of 23,000 miles. Because of its stationary position, it is always in communication with its ground station. This has a substantial effect on the complexity of the command systems. Only the command about to be executed need be stored at any one time.

The satellite weighs about 760 lbs. and is designed for an active life of three years. The electronics consists of two identical subsystems to achieve reliability through redundancy.

Figure 3 - 2 shows a portion of the Syncom system. This contains two sections, the PFM telemetry section and the command section. These subsystems are not directly associated with the communication relay function but serve to monitor the conditions of the satellite and perform station-keeping duties. There are 120 telemetry channels; these are commutated to appear on one line, pass through a level limiter and to a sub-carrier oscillator. The commutation is accomplished in the dotted area which includes a nine-stage transistor binary counter and an 8 x 16 matrix. The matrix includes the logic to decode the counter and also handles the signals to be telemetered. All signals must pass through two gates to arrive at the output. It should be noted that the highest frequency involved with the counter and matrix-gate is less than 200 cycles.

The command section looks much like the dotted telemetry section in reverse. The one line from the command receiver is expanded to 64 lines at the output of the command matrix. Much like the telemetry section, a binary number in the counter-shift register is recognized by the matrix as representing one command out of 64. For backup in case of a failure the command section can operate either by shifting in the right binary number or counting to that number. Again, the frequencies encountered are easily handled by any of the present microcircuits.

In addition, Syncom contains a large amount of electronics in the microwave repeater - receivers, antenna phase sensors and drivers, traveling-wave tubes and transmitters. Naturally, the power supply, converters and regulators are sized for this larger task. The command subsystem is shown in Table 3 - 4.

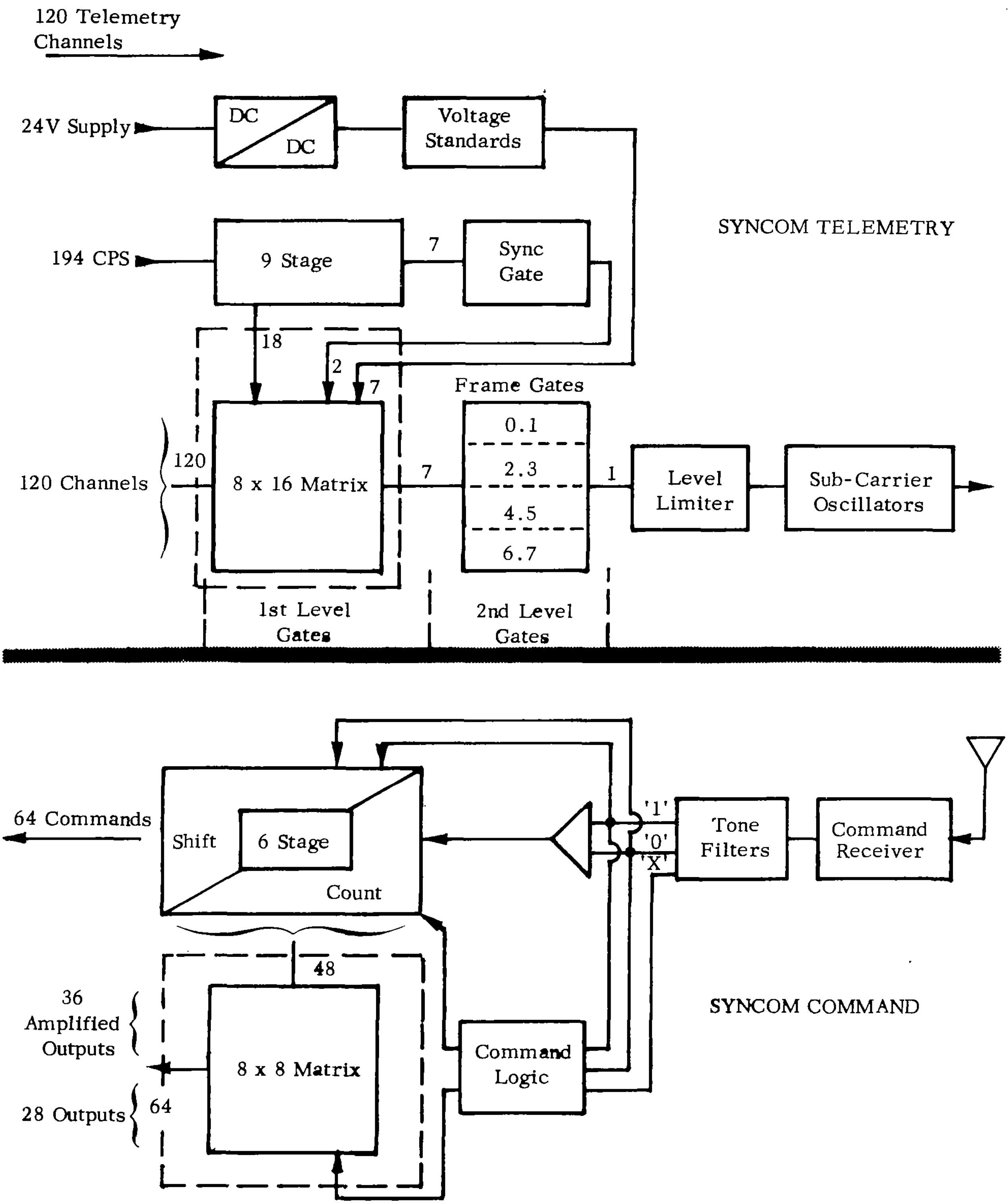


FIGURE 3.2 SYNCOM TELEMETRY AND COMMAND SUBSYSTEM

TABLE 3 - 4

SYNCOM A COMMAND SUBSYSTEM DATA

64 Commands	Volume cu. in.	Weight lbs.	External and Component Connections	Power mw.
Total Subsystem	280	1.7	400 + 2572	1300/3500
Per Command	4.4	.027	46	20/50

C. NIMBUS

This satellite has been designed to supersede the TIROS weather observatory satellite, intended to provide more complete meteorological observations from a 500 mile high orbit.

The infrared and visual sensors, TV cameras and data transmitters are functionally separate from the telemetry and control subsystems. Only the latter are discussed here. The functions of these are to provide sensing and transmission of "housekeeping" data on satellite conditions such as voltage and temperature levels, and data on the space environment, spacecraft attitude, and clock time. The control receiver must provide signals for attitude correction whenever necessary.

Because of the nature of the Nimbus satellite, its orbit and job to be done, the telemetry and command is more complex than that of Syncom. There are times in its orbit that it is not available to ground control and yet certain functions must be carried out. This requires a program of stored commands that can be executed at the precise time required. The TV camera portion of the satellite has not been included in this study.

Figure 3 - 3 illustrates the Nimbus telemetry and command subsystems. There are two separate telemetry sections. The "A" unit stores its data on a tape recorder and is later played back when commanded to to so. The "B" unit, on radio command, commutates once through 128 input channels.

Both telemetry sections are assembled from the same basic building blocks. The blocks are magnetic core shift register stages. The "A" unit has 544 input channels; some of these are sub-commutated channels; the "B" unit has 128 inputs.

Again, the speeds encountered are well below the capability of most microcircuits. Only the A/D converter uses a 200 KC bit rate. In block form the dotted area shown in Figure 9 resembles the same section shown dotted on the Syncom diagram of Figure 3 - 3.

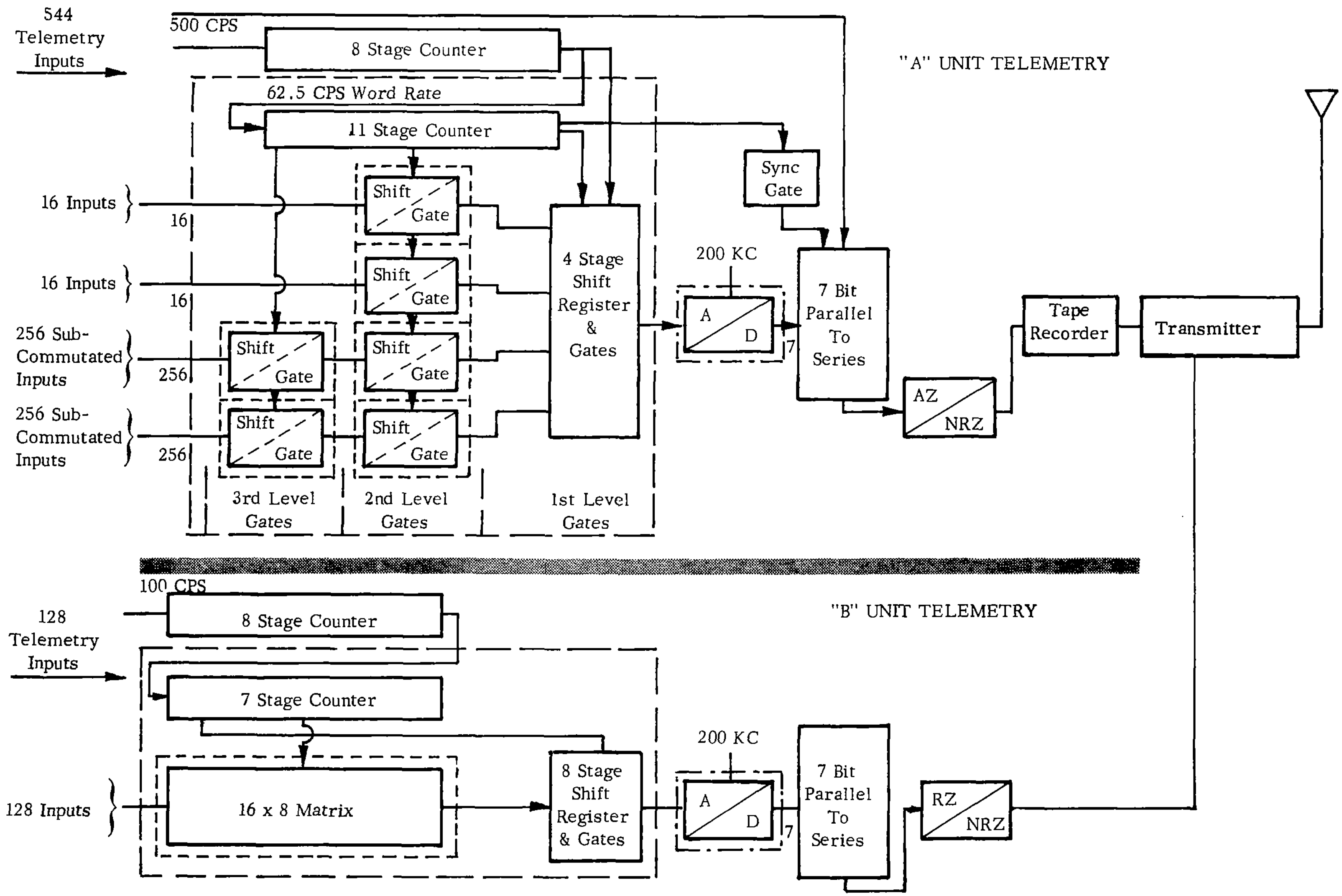


FIGURE 3.3 NIMBUS TELEMETRY SUBSYSTEM

D. THE OBSERVATORY SATELLITES AND THEIR COMMUNICATION AND DATA HANDLING SUBSYSTEMS

The functional design and major components of the communication and data handling subsystems for the three observatory satellites, OGO, AOSO, and OAO are reviewed individually. Integrated circuits have already been of value in the AOSO program. In addition to being able to achieve similar advantages with the other observatory satellites, a degree of standardization of subsystems is also possible between these three and other satellites.

OGO

OGO is the earliest of the three satellites. Its first launch is scheduled for mid-1964. Its size is roughly 3 feet by 3 feet by 6 feet. Its total weight is 1,000 pounds, including the capacity for 150 pounds of experiments. It is intended that the OGO series of satellites will have elliptical orbits. In one case (EGO) the orbit will range from 150 to 6,000 miles. In another case (POGO), it will range from 140 to 500 miles. A block diagram for OGO appears in Figure 3 - 4. The OGO satellite like the remaining two observatory satellites can be seen to consist of fundamentally four independent systems. They are: the command and control system, the tracking beacon system, the system clock and the data handling and telemetry system. The command control system can be seen to include two command receivers operating in parallel and designed so that if either one fails the gain of the other will be doubled. The outputs from the two receivers are combined to drive the command decoders. There is one tone decoder which is operated in real time and is included as a backup in the event of failure in the digital decoder section. The tone decoder has capacity for up to 15 commands. The combiner and detector also drives two parallel digital decoders which in turn drive a command distribution unit. Two digital decoders are provided with one acting as a redundant unit in the event of a failure in the first. The bit rate for commands in OGO is 128 bits per second. Only real time commands can be handled by OGO since no command storage is provided. The command word for OGO is 32 bits, providing a total of 254 possible digital commands. Of these 104 are commands pertaining to satellite systems while the remaining 150 pertain to experiment systems.

The beacon subsystem can be seen to consist of two 100 milliwatt beacons and one 10 watt beacon. Normally one, but only one, of the 100 milliwatt beacons is transmitting. The second unit serves as a backup and can be switched in under command control. The 10 watt beacon can also be switched in under command control when necessary for reliable tracking at long ranges. It is switched in for 45 second intervals during which the other beacon is turned off.

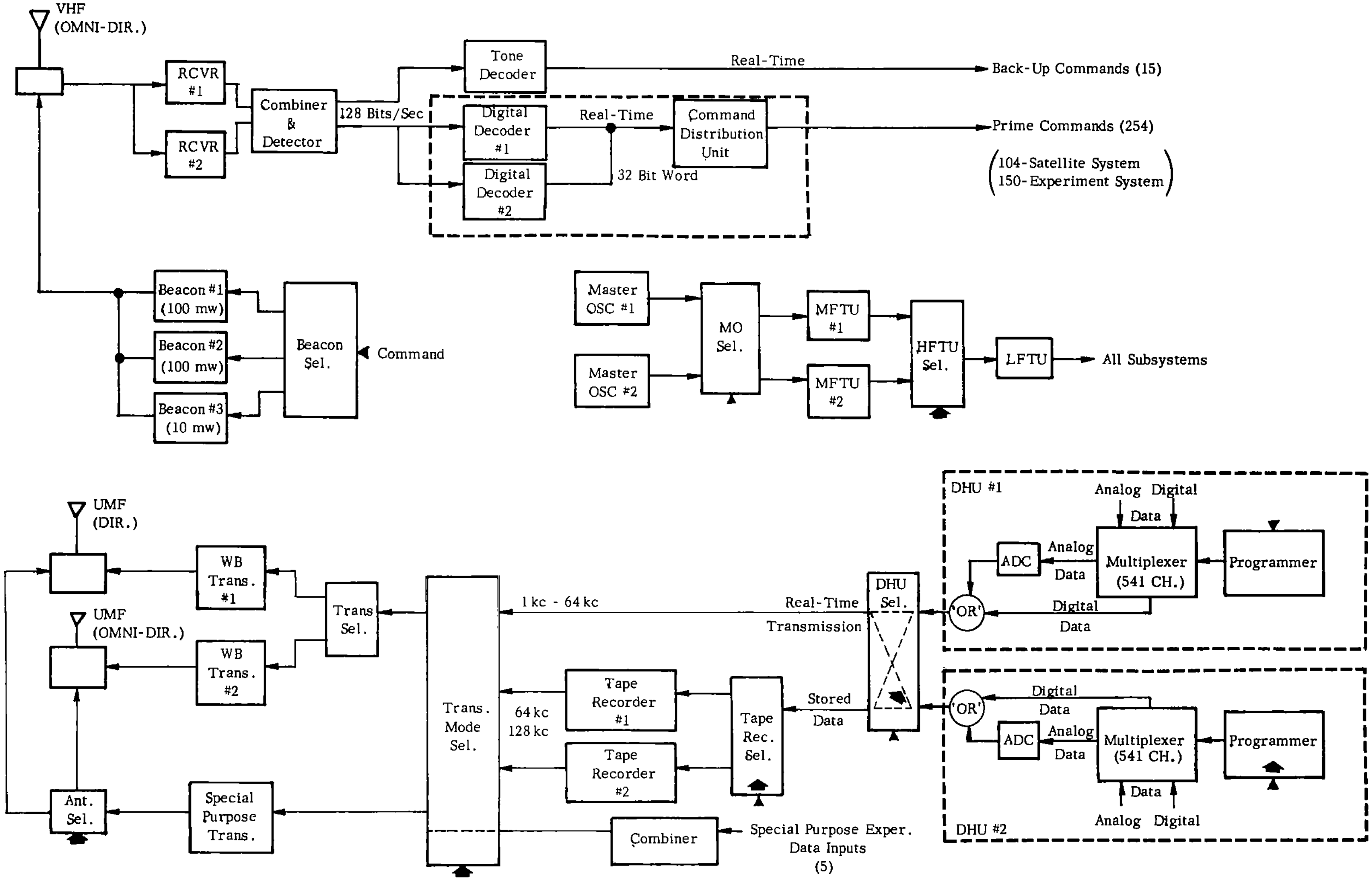


FIGURE 3.4 OGO COMM. AND DATA HANDLING SUBSYSTEM

The timing system for OGO as for other satellite systems consists of a master oscillator and a binary countdown change to provide the many frequencies needed by the satellite systems. In OGO two master oscillators are provided either of which can be selected by command control in the event of failure of the other. The selected master oscillator drives one of two high frequency timing units which provide many of the frequencies needed by the satellite systems. Again two high frequency timing units are provided, one as a backup for the first. The output of the high frequency timing unit drives a final low frequency timing unit which provides additional frequencies for some of the subsystems. Only one LFTU unit is provided in OGO.

The next and largest part of this subsystem is the data handling and telemetry subsystem. Two completely independent data handling units are provided in OGO. Each includes a multiplexer, an analog-to-digital converter, and some circuitry for controlling the format of sampling under command control which is called the programmer. Each of the two data handling units sample essentially the same inputs. That is, they are operating essentially in parallel. One of the two data handling units drives a transmitter for real time transmission while the other drives a tape recorder. The roles of the two data handling units can be interchanged under command control. Two tape recorders are provided, one serving as a backup for the first. Under command control either one of the two can be selected for recording the generated data. The stored data can be read out under command control into the telemetry transmitters for transmission back to earth when desired. Two wide band transmitters are provided for telemetry transmission. Again, either one can be used, never both. A minor consideration for our purposes is a third transmitter which is called the special purpose transmitter. This transmitter is included to transmit data from a few special experiments whose outputs are incompatible with the time sharing or sampling feature of the digital system.

It should be noted that the bit rates or operating speeds for the digital circuits in OGO are relatively low. The command control subsystem operates at a bit rate of 128 bits per second. The data handling subsystem operates at significantly higher speeds but at speeds which are still low with respect to what is normally available in conventional and integrated circuit modules. The bit rate for the data handling subsystem can range from 1 KC to 64 KC under command control. The maximum output rate from the tape recorders is 128 KC. It is reasonably safe to say that, excluding the highest stages in the clock countdown unit, the highest bit rates of interest are in the order of 100 to 200 KC.

OAO

The OAO satellite is the largest of the observatory satellites. It is approximately 10 feet long and 80 inches in diameter. Its weight is 3600 pounds including 1000 pounds for experiments. It is scheduled for launch late in 1965 and will have roughly a 500 mile orbit. Functionally, OAO is very similar to OGO with one major exception. That is, OAO has a capability for storing commands for execution at a later time. Again, however, one can see in Figure 3 - 5 that the OAO communication and data handling subsystem consists of the same four basic boxes. To repeat they are the command control, the beacon, the system clock, and the data handling and telemetry subsystems. OAO includes four command receivers operating in pairs off two antennas for omnidirectional coverage. Again, either one of the two receivers in each pair can fail without interrupting the operation of the system. The outputs of the four receivers are combined and detected to drive the command decoding and distributing units. The command bit rate for OAO is 1042 bits per second and again the command word is 32 bits long. Apparently only one command decoder is provided. No doubt there is some redundancy provided, particularly in view of the fact that no tone decoder is provided as a backup. Real time commands are distributed immediately while non-real time commands are fed to the command memory and programming unit where they are retrieved at the proper time and fed to the command distributor. OAO has sufficient command storage for 128 individual commands. It is our impression that the total number of commands is less than 256.

The beacon subsystem for OAO includes two beacon transmitters, either one of which is continuously transmitting. The second can be switched in under command control in the event of the failure of the first.

The system clock for OAO includes a master oscillator and countdown chain. While we are not aware of any redundancy in this area, we expect there probably is.

Unfortunately we have not been able to collect very much detailed information about the data handling and telemetry subsystem for OAO. We do know, however, that two individual data handling systems are provided. One samples and processes spacecraft data while the second samples and processes experimental data. Both are controlled by a rather extensive programmer which operates under command control and both have access to data storage. The spacecraft data is processed at relatively low bit rates, 1042 bits per second. The experimental data is processed at a substantially higher rate, 50 KC. The spacecraft data is transmitted via one of two narrow band transmitters while the experimental data is transmitted by one of two wide band transmitters. The second transmitter in each case is provided as a backup to the first and can be switched in under command control. The data storage in both the command memory unit and the data handling units consists of dual aperture ferrite cores for non-destructive read out. In the command memory, the information is stored in four separate locations for

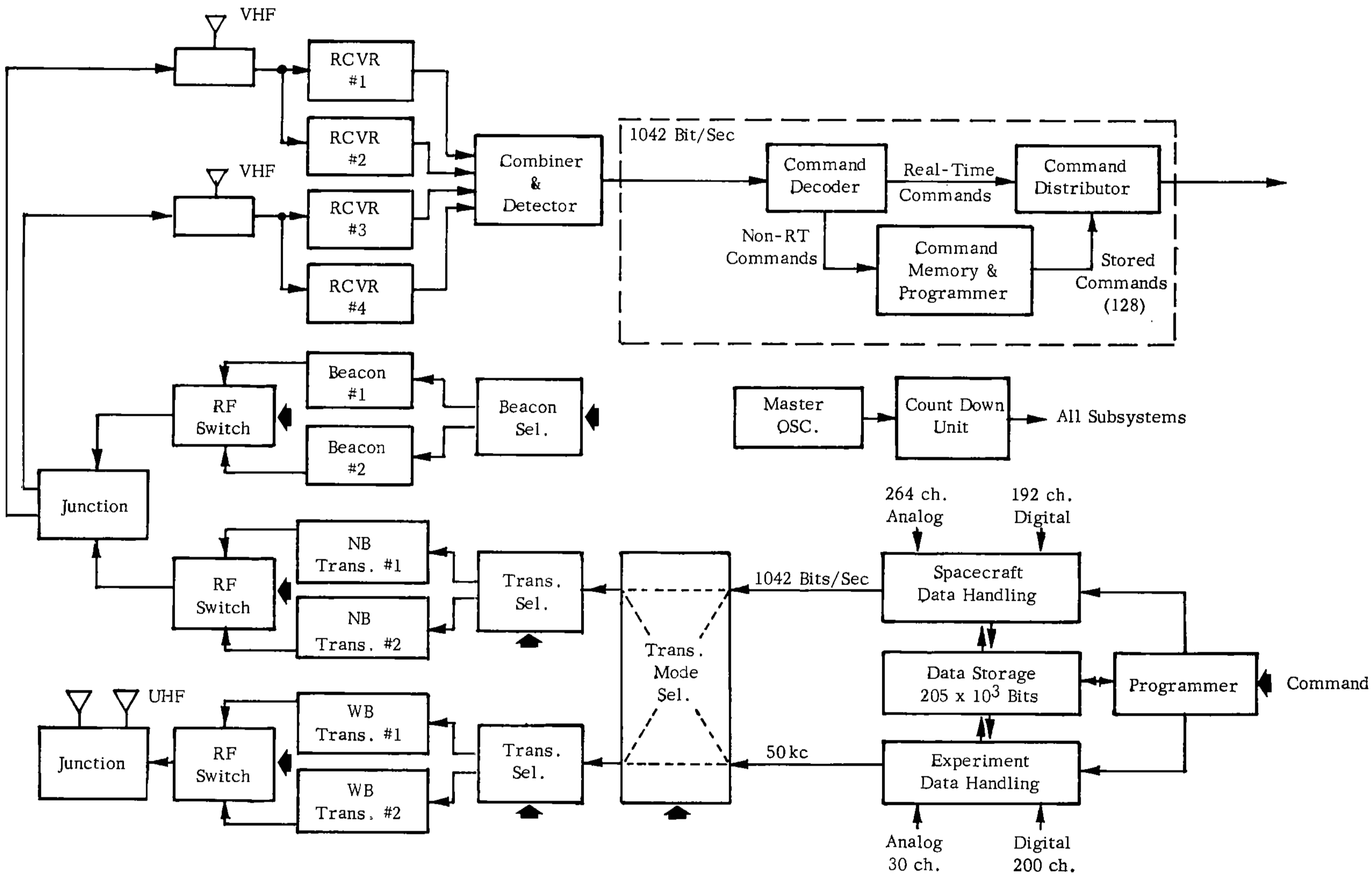


FIGURE 3.5 OAO COMM. & DATA HANDLING SUBSYSTEM

redundancy. Two independent data storage units are provided. The two can be operated either independently or in parallel for redundant operation.

Again, we see that the bit rates involved in the command and data handling areas are quite low. It certainly appears that the bulk of the digital logic operates at speeds below 200 KC.

AOSO

While we were not initially planning to include the AOSO satellite in our initial assignment, we did so for two reasons. First, it completes the picture for the presently planned observatory type satellites. Second, it affords the opportunity to observe the improvements that can be gained by the use of integrated circuits in certain areas. The AOSO satellite is now in the design stage and is scheduled for launch in 1967. The design of the communication and data handling subsystem is being done by Texas Instruments who have chosen to use integrated circuits for all digital logic functions. All analog circuits including the analog transmission gates will be designed using standard components. The AOSO satellite is similar to OGO in many respects. Its total weight will be 1000 pounds including 250 pounds for experiments. It will be approximately 10 feet long and 40 inches in diameter and will fly a 300 mile orbit.

Looking at the block diagram for AOSO in Figure 3 - 6, it can be seen to be quite similar to OGO, with of course some exceptions. Again, one can recognize the four basic subsystems. Four command receivers will be provided in AOSO operating in pairs off two antennas. The combiner and detector drives a tone digital decoder in addition to the PCM digital decoders. The tone digital decoder will be provided as a backup and will have capacity for 30 to 70 commands. Present plans call for two PCM decoders although consideration is being given to providing a third. Only one is needed, the other one or two will be provided as backup in the event of failure of the first two. Any one of the decoders can be selected under command control. The AOSO satellite like OAO will include command memory for storage of non-real time commands. Real time commands will be executed immediately through the command routing unit while non-real time commands will be stored and retrieved at a later date. The command bit rate for AOSO is 512 bits per second. The command word is 32 bits and the command capacity is 254.

Two beacons are provided for tracking. One of the two units will operate continuously. The second unit will be switched in under command control in the event of failure of the first. Two completely independent system clocks will be provided in AOSO. Either one can be selected under command control.

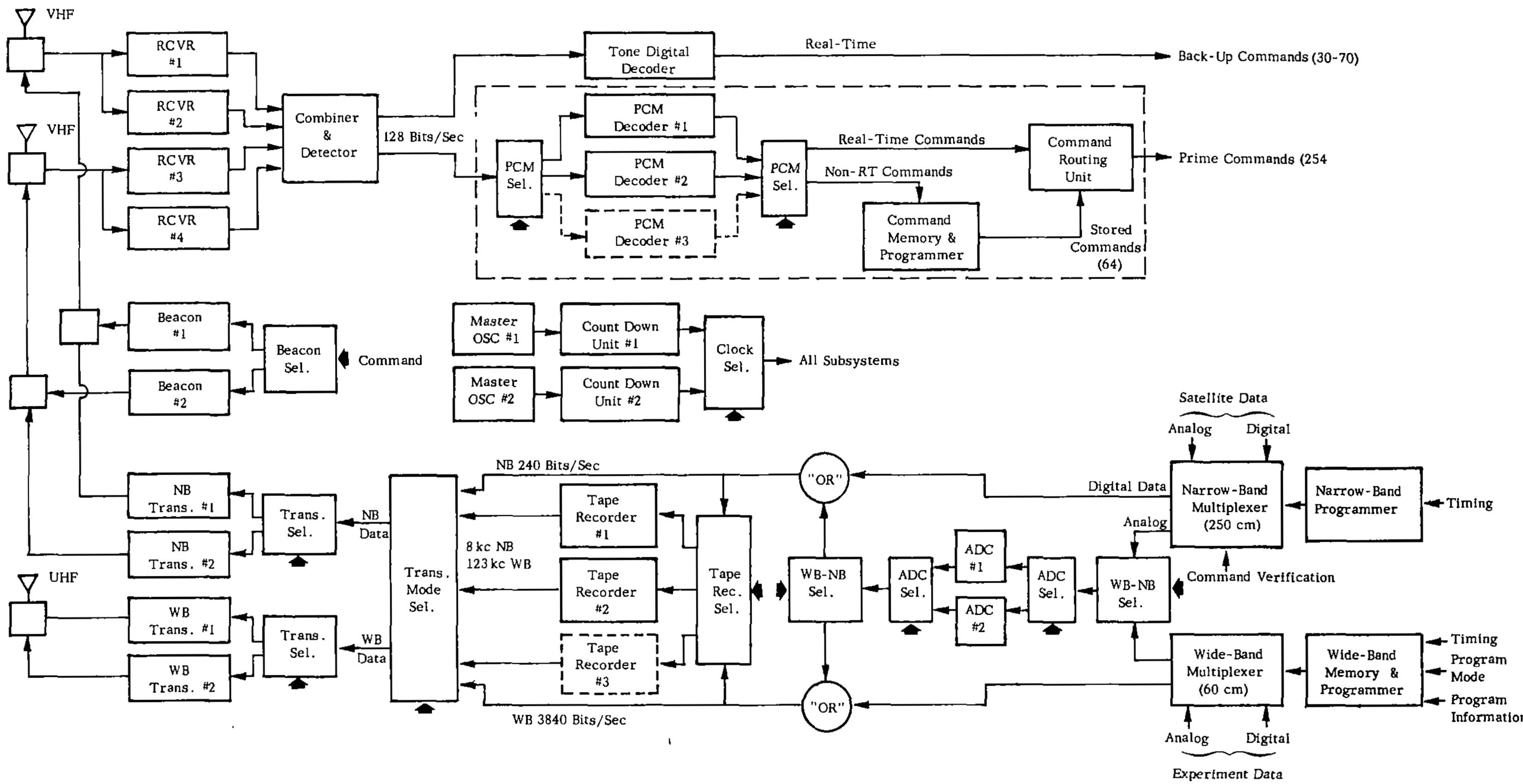


FIGURE 3.6 AOSO COMM. AND DATA HANDLING SUBSYSTEM

The data handling and telemetry portion of AOSO includes two multiplexers with individual controls, two analog-to-digital converters, two tape recorders (possibly three) and four telemetry transmitters. Two of the transmitters are narrow band and will be normally used for satellite data while the other two are wide band and will normally be used for experiment data. One multiplexer samples 250 channels of satellite data, while the other samples 60 channels of experiment data. The analog-to-digital converter and tape recorder will be time shared between the two multiplexers. Only one tape recorder will be used at a given time but redundant units are provided as backup. Looking at the data rates involved, we see that the narrow band data handling bit rate is 240 bits per second while the wide band data handling bit rate is 3840 bits per second. The output bit rate from the tape recorder will be 7680 bits per second for narrow band data and 122,880 bits per second for wide band data. Again, it is clear that the bit rates involved are relatively low, certainly below 200 KC in both cases.

Now that we have described the three observatory satellites, we can see that while many similarities exist there are also differences between the three. Some of these differences are in the methods provided for insuring reliability through redundancy. In general, the approach to improving reliability by redundancy is to provide redundant major subsystems. That is, a completely independent transmitter is provided or a completely independent decoder or a completely independent data handling unit. We can see that AOSO has gone further in this respect than the other two. This is in part a fringe benefit of using integrated circuits since their much smaller volume and weight makes it possible to include more circuitry in the same box. This is an oversimplification, however, because the resulting power requirements will increase with a resulting increase in the power system. AOSO affords us an excellent opportunity to determine the advantages that might be gained through the use of integrated circuits in systems like these. As indicated earlier, AOSO is presently in the design phase and will use T.I. integrated circuits for all digital logic. The present design can, therefore, be compared with earlier estimates, Table 3 - 5, made for AOSO using conventional components. It can also be compared with OGO which is quite similar and which preceded AOSO by a few years.

TABLE 3 - 5

AOSO MODULE BREAKDOWN

	Flip-Flop	Dual 2-input NAND	8-input NAND	Dual 2-input NOR
Total Modules	474	486	131	36
Components/Module	18	10	10	10
Total Number of Components		15,000		
Total Internal Connections		33,000		
Number of Different Components		15		

Note: This table lists discrete version now superseded.

E. COMMON SUBSYSTEMS

From the description and an analysis of the diagrams for these satellites, certain types of subsystems have been identified which represent areas where some standardization may be possible. In this case additional advantages might be gained through the multiple use of such common subsystems as are shown in Table 3 - 6. Restricting ourselves to the three observatory satellites for the moment, there is one large sub-assembly which appears to be reasonably common to the three. That sub-assembly is the command decoding and routing system. While there are some differences in these three systems particularly with respect to redundancy and command storage, the basic function that must be performed in this sub-assembly is the acceptance of a command word, decoding of the command word, and control of a command matrix. That is, given an 8 bit word, one must energize one of 256 outputs. The bit rates in all three cases are very low, the command word in all cases is 32 bits and the total number of commands is the same. This, therefore, may be an area ideally suited to the development of a standard sub-assembly using integrated circuits. This same type of sub-assembly may find additional use in these satellites and other satellites in the data handling and telemetry portions. The function that must be performed there is very similar; that is, given a parallel binary code in a counter one must energize or activate a specific transmission gate in a cluster of many. While the size of the matrices or the number of channels varies from one satellite to the other, it seems reasonable to assume that the required number of channels could be provided by stacking up a group of smaller standard boxes. Another very obvious common box to all three is the analog-to-digital converter. While this unit also involves analog circuitry, it may be desirable to provide a standard sub-assembly using integrated circuits to perform the digital logic operations that are required. Finally, there are certainly many smaller and more obvious common boxes to each of these satellite systems. These might include things like shift registers, counters or combination shift and count registers.

TABLE 3 - 6

COMMON SUBSYSTEMS

Encoder

Command Decoder

Analog-to-Digital Converter

Counter

Shift Register

Multiplexer

Voltage-Controlled Oscillator

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During the early phases of the study the current literature was scanned in order to obtain published information on the circuits, the block diagram and the component content of the selected spacecraft electronic systems. A considerable amount of background information was available from current literature on those which have been designed some time ago. On the more recent type satellites, such as IMP, extremely little published information could be obtained.

A selected list of those references, which contained at least some portion of the information suitable for this microelectronics study, has been compiled and is presented herewith.

Upon completion of this initial briefing from the current literature, a number of visits to GSFC were made by our staff. The applicable project documents, interface diagrams, and relevant circuit drawings were inspected and obtained through the courtesy of the project managers and the director of GSFC. Those which have been particularly useful during the performance of this study are also listed.

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IV. TASK 2 - MICROELECTRONIC CIRCUIT ANALYSIS

A. CHARACTERISTICS

The characteristics of a variety of silicon integrated circuits have been derived from the manufacturers' specifications, and only those deemed most suitable for medium-speed low power operation have been investigated in more detail. Table 4 - 1 lists a number of types of integrated circuits readily available now, but omits others more suitable for high speed, high power use. This refers to a comparison of simple 3-input gates, which are one of the very basic building blocks of digital circuits. Frequently, emitter followers or additional inverters are included with such gates, both slowing down the response slightly and increasing the power requirement.

Referring to Table 4 - 1, a semiconductor integrated circuit, as used here, is a monolithic device such as a gate or a flip-flop which is constructed on a single chip of silicon. A discrete module or "standard" circuit is a similar circuit, of comparable operating characteristics, constructed of conventional components and packaged in as small a form as possible, usually encapsulated in some material to form a module. The table shows some of the integrated circuits manufactured with some performance figures of these products. The first four are the oldest manufacturers in the field and have a generally wider variety of types of devices and wider range of available power and speeds. The last row contains several manufacturers whose products are reasonably similar and who have entered the field more recently. They are also representative of a large number of other manufacturers who are not listed here. Attention has been focused in particular on the generic types represented by the Texas Instrument Series 51 and the Fairchild Milliwatt Micrologic, since most of the satellite applications studied here do not require any great speed but do require as low a power consumption as possible. The two manufacturers, Texas Instruments and Fairchild, have the lowest power devices available on a standard off-the-shelf basis, although others, CBS for example, have designed lower power types of specialized design. The types of logic circuits readily available in low power form are either resistor coupled transistor logic or diode transistor logic. Of the first four manufacturers, listed in Table 4 - 1, T.I., Fairchild and Motorola use the resistor coupled transistor logic and Westinghouse uses diode transistor logic.

There are, in general, two types of packaging available, the flat pack and the modified TO-5 round metal case. The flat pack offered by many has very small volume. That of Texas Instruments and a few additional manufacturers offer the smallest available. There also exists a slightly larger one which has been adopted by Westinghouse as well as other manufacturers. The modified TO-5 can is being used by Fairchild and Motorola and a number of additional suppliers, and some small circuits are also offered in smaller round cans such as the TO-18 package. However, it is generally true that any integrated circuit can be obtained in any type package desired on a special order with no major change in price or change in any of the significant electrical parameters, except for the package price, weight and volume. The power consumption of these selected integrated circuits (T.I., Fairchild, etc.) shown is 2 milliwatts at 3 volts. In most applications they may possibly be operated at a higher voltage to provide a circuit with wider margins for additional reliability. However, they are specified to operate at 3 volts and the figure of 2 milliwatts is used here in Table 4 - 1 as the minimum power consumed by these "ordinary" integrated circuits. Many manufacturers now offer other types which are much faster, operating at 5 to 8 megacycles clock frequency and about 10-15 milliwatts of power. Such devices as are generally available appear functionally quite similar. They all offer a flip-flop which can be connected either as a counting flip-flop or as a shift register. They offer a selection of at least two types of gates; a many-input gate, the maximum being of the order of 6 inputs NOR or NAND; and a dual 2 or 3 input NOR or NAND gate. In addition to these there generally are available some much more complex devices, usually designed from a combination of these two basic gates mentioned. There are also buffers available for extending the fan-out of these devices, or else alternate versions with a built-in emitter follower or amplifier, which allow a fan-out of up to 20.

TABLE 4 - 1

INTEGRATED CIRCUIT - PERFORMANCE FIGURES

		Weight of Device	Equiv. Weight on Circuit Board	Volume of Device	Equiv. Volume on Circuit Board	Power	Fanout	Speed	Type of Logic
TI Series 51 - Flat Pack		0.1 gm	0.5 gm	0.0025 cu. in.	0.025 cu. in.	2 mw @ 3 V	5 or 20 with E.F.	500 KC	RTL
Fairchild Milliwatt Micrologic	TO-5 type	0.7 gm	1.1 gm	.024 cu. in.	.08 cu. in.	2 mw @ 3 V	4	1 MC	RTL
	Flat Pack	0.25 gm	0.9 gm	.011 cu. in.	.04 cu. in.				
Westinghouse Functional Electronic Blocks	Flat Pack	0.25 gm	1.1 gm	.011 cu. in.	.04 cu. in.	20 mw @ 6 V	4	9 MC	DTL
Motorola MECL Integrated Circuits	TO-5 type	0.7 gm	1.1 gm	.024 cu. in.	.08 cu. in.	35 mw @ 5.3 V	26	20 MC	RTL
Amelco; General Micro-electronics; Signetics; Siliconix; Sylvania		Both TO-5 type and .011 cu. in. Flat Pack				3 mw to 15 mw	4-5 or 15-20 with E.F.	1-2 MC	DCTL and DTL

Source: Company product literature

Note: E.F. = Emitter Follower

B. "IN-CIRCUIT" PERFORMANCE

It may not be sufficient in the preliminary design of a system to take the values from Table 4 - 1; rather a conservative multiplier may first have to be applied to complete the assessment to allow for buffers, inverters and so on.

Not only is the performance of a more elaborate circuit slower and draws more power in return for its greater drive capacity and margin, but also one must consider similar effects on cost, weight and volume. Table 4 - 2 shows the comparison of integrated circuits with discrete circuit modules of similar performance.

From this table we see that an integrated circuit package is about 50-fold smaller than a corresponding discrete module. Yet we have not yet learned to shrink our printed circuits and chassis by the same extent. Thus, a printed board, chassis, and equipment, will have a lesser drastic though still major reduction in weight and volume when using integrated circuits.

Table 4 - 2 shows in summary a comparison of integrated and discrete circuits. The "standard" discrete circuit represents an approximation to the size and volume of available standard modules of discrete components. The power is an indication of what one could obtain having designed for the same speed of operation as the standard integrated circuits that are available. With special circuits tailored for a specific application this power figure can probably be lowered to a half milliwatt or possibly less. However, this figure was taken as an indication of the power a standard line of modules, capable of 500 kilocycle operation, would require to operate reliably. The first two lines of this table list the weight, volume and power of the integrated and standard circuits on their device or module level. The next two lines give the effective weight and volume which pertains to a single module or integrated circuit after having been mounted on a circuit board and a number of these connected together. The fifth and sixth lines give the multiplier from an isolated device to the device on an actual circuit board. On mounting on a board, there is a five-times increase in weight and a ten times increase in volume for an integrated circuit, contrasted with a 1.2 to 1.6 increase in weight and a 1.2 to 2 increase in volume of the heavier and larger standard circuit. Thus, there still exists a 10 - 20 times saving in weight and a 20 - 30 times savings in volume when integrated circuits are used in place of standard circuits at the circuit board level.

When these devices are mounted in a chassis an average figure for the "per module" weight and volume would be about 10 grams or 1.2 to 1.7 times the weight on boards and a .7 to 1 cubic inch volume or 1.2 to 2 times the volume on boards. For integrated circuits mounted

TABLE 4 - 2

COMPARISON OF INTEGRATED AND STANDARD CIRCUITS

	Failure Rate %/1,000 hrs. @ 25°C	Weight (grams)	Volume (cu. in.)	Power (m.w.)
Integrated Circuits - Device Level	.003	.1 gm	.0025	2
Discrete Circuit Modules	.004	5 gm	.4	1
Integrated Circuits on Boards		.5 gm	.025	2
Discrete Circuit Modules on Boards		6-8 gm	.5-.8	1
Multiplier for Integrated Circuits		5	10	N.A.
Multiplier for Discrete Circuits		1.2-1.6	1.2-2	N.A.
Ratio Between Mounted Integrated Circuits and Discrete Modules		10-20	20-30	½
Discrete Circuit in Chassis		10 gm	.7-1.0	1
Integrated Circuit in Chassis		0.5-1.0	.035-.050	1

Note: Failures from 1963 fourth quarter data.

in a chassis, there is an increase of from 1 to 2 times in weight and from about 1.4 to 2 times increase in volume. This does not affect the ratios very much, still giving the integrated circuit a ten to twenty weight advantage and a twenty to thirty times volume advantage over standard circuits.

Figure 2 - 2 may also be used to infer this in a more general way. It is shown that flat-pack silicon integrated circuits have a capability of 20 million components or 700,000 circuits per cubic foot, but that present packaging methods on circuit boards with some space left for welds and the separation of boards provides a density of "only" 1.5 million equivalent components or 70,000 circuits per cubic foot. This is still a greater density than one can utilize at present. The weight savings, which are actually more important in spacecraft electronics, are also considerable over discrete components. Again, the advances possible from integrated circuits have temporarily outstripped our present packaging techniques.

C. MODIFICATION OF PRESENT UNITS

Unfortunately, the integrated circuits now available will generally consume more power than available designs of otherwise comparable discrete circuits designed to perform the same function. Fortunately, most telemetry systems of present satellites are operated at data rates or at frequencies much lower than the 500 kilocycle to 2 megacycle maximum speed capabilities of the cited integrated circuits. There would be a great deal of room for units having less frequency capability with the lower power consumption which would then be possible.

Figure 4 - 1 shows the range of clock speed and power drawn for an illustrative circuit, a simple NAND gate of a number of available types. The power drawn per megacycle of frequency can be used as a figure of merit for comparing integrated or standard circuits. It describes the relationship between the speed and power consumed by the circuit. Although at the present time most discrete circuits are operating at 2 milliwatts per megacycle or above, values under ¼ are within the state of the art.

The speed-power capability or figure of merit has been improving with time, as shown in Figure 4 - 2. This has resulted from the increasingly improved understanding of the problems of parasitic capacitance in integrated circuits and their gradual solution. To date, the reduction in power per unit of clock frequency (i.e., a shorter propagation delay at given power) has been achieved through a reduction in size of the diffused transistor components, and an increase in silicon resistivity permissible through the use of epitaxial techniques. Further substantial improvements are expected to follow from the use of the newest dielectric isolation techniques.

Since all this speed capability may not be necessary in the applications here considered, one can trade off speed for power consumption and design devices for micropower operations, such as some prototype CBS devices operating at around 10-20 microwatts at about 10 kilocycles. These were developed under other NASA programs. On request, integrated circuit manufacturers could, within three to six months, develop a series of integrated circuits which will operate at 100 to 200 microwatts, suitable for a 50 kilocycle clock rate. Such devices could be used in the majority of the satellite telemetry applications presently considered here. However, a comparable discrete "standard" circuit designed to operate at 50 kilocycles could still be designed for lower power operation than the integrated circuit. Because of the low speeds being used, the integrated circuit components need no longer be treated as completely distributed elements, and some parasitic capacitance effects which tend to limit high frequency response are not as important at these low frequencies, even though they do affect performance in contrast with isolated transistors. A series of integrated components comparable to the types now manufactured by the major suppliers, designed for these low power levels, would be very useful building blocks for the applications satellites studied here.

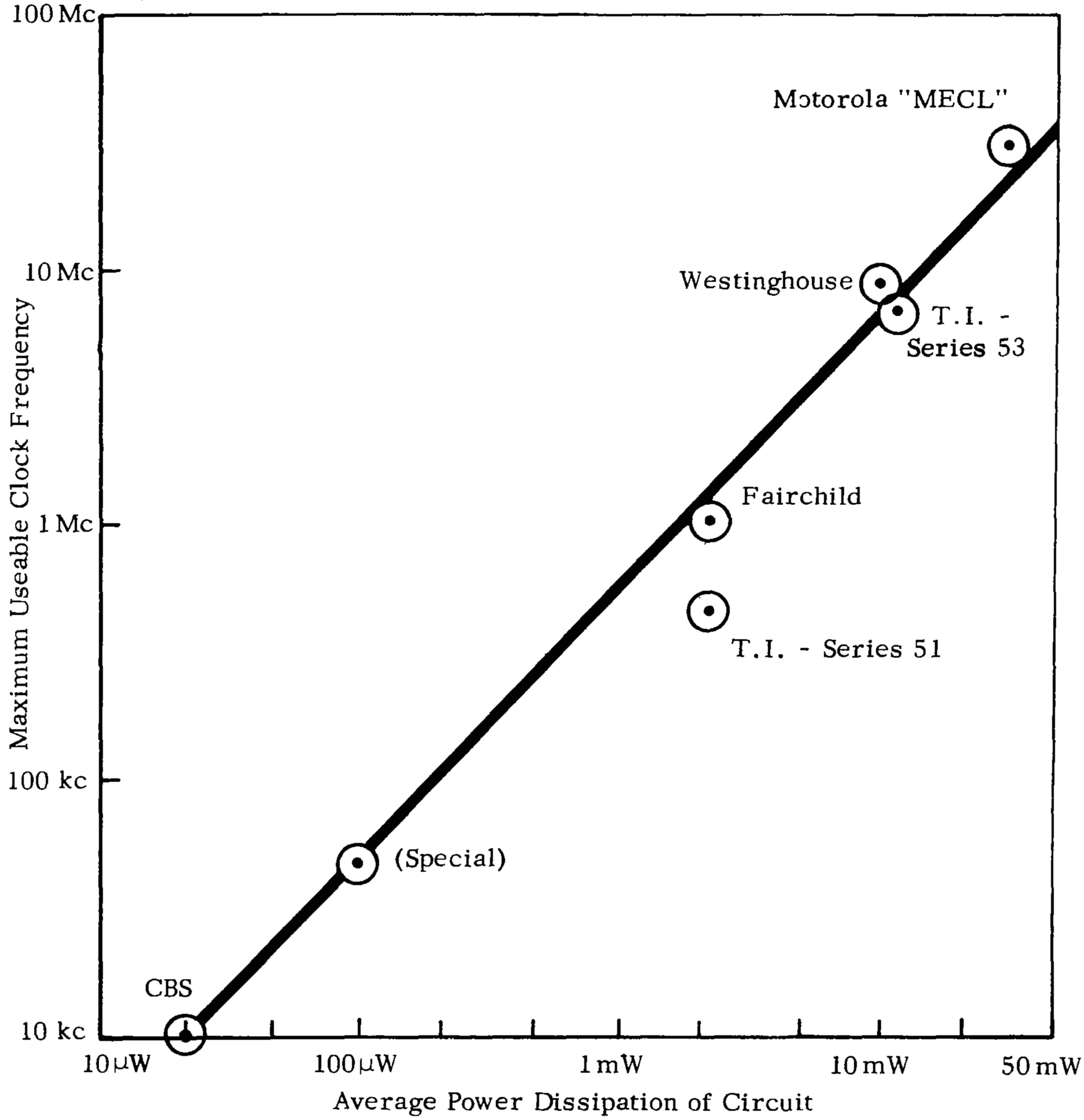

FIGURE 4.1 SPEED-POWER RELATIONSHIP (1963)

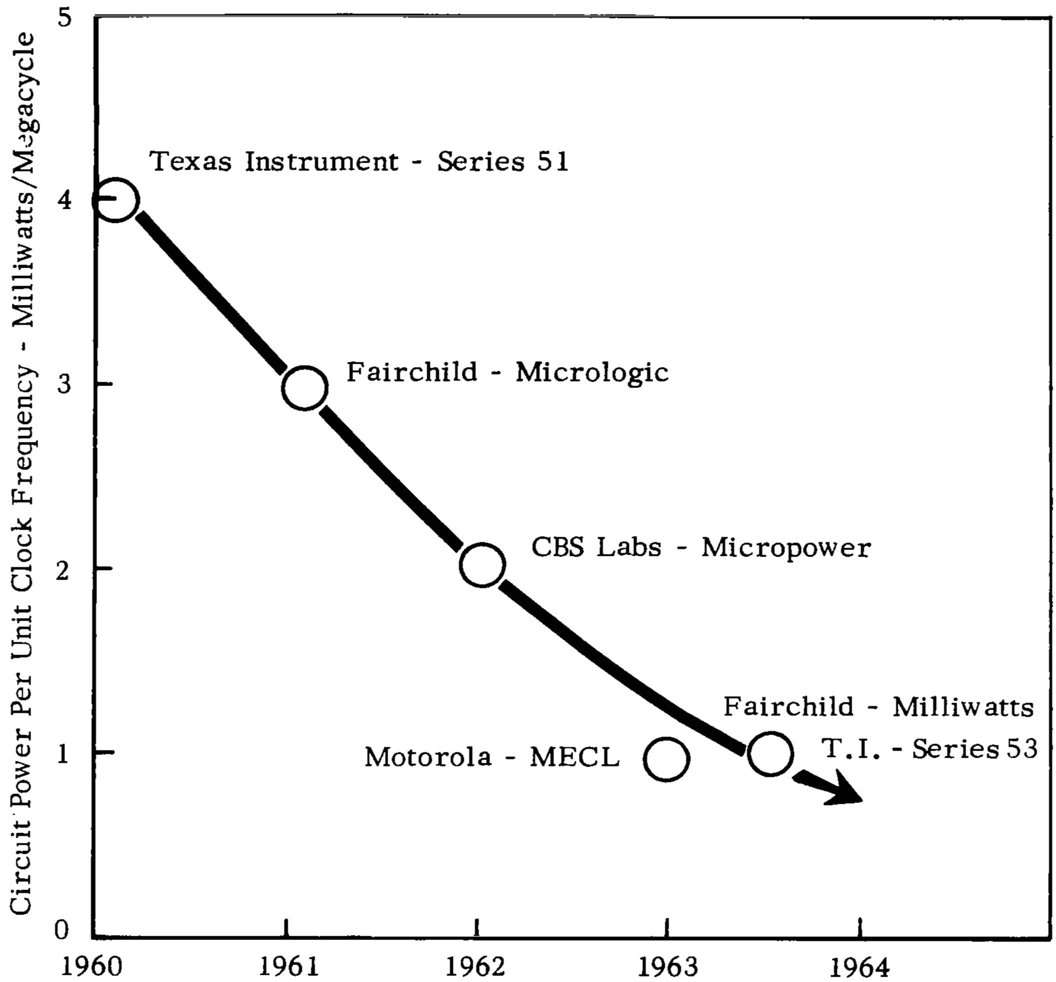

FIGURE 4.2 TREND OF INTEGRATED CIRCUIT POWER AND SPEED--NAND GATES

D. MULTIPLEXERS

Functionally, the spacecraft systems outlined here share certain subsystems. One of these common subsystems is the multiplexer. Such subsystems may have other names, but the multiplexing function is common among all the different satellites, even though the individual block diagrams differ.

A more detailed discussion of the multiplexer shows how this, in turn, can be built up from a number of elements such as counters and registers, and how it can be applied both to encoding and decoding.

In Figure 4 - 3 we have depicted a general block diagram to illustrate the multiplexing function. On one side is the prime signal gate matrix. This matrix consists of a collection of analog and digital transmission gates which handle the various signals from all the experiments, the spacecraft housekeeping data, and all the separate signals which are to be passed to the telemetry. In response to certain control signals, one or more of these gates close at a time, and they are all sequentially sampled. The data is fed in on the lines marked analog-digital data "in" and fed back out again on a single line (or possibly two lines), represented here as digital lines "out" and analog lines "out". The third line is a "data mode" line which indicates whether the data signal is in analog or digital form.

In general, there is no pattern common to all spacecraft as to how the analog and digital signals are divided. In any given spacecraft, however, there will be a pattern, and it is reasonable to assume that a standard pattern could be assigned which would permit these gates to be assembled in blocks; the blocks then in turn could be put together to form the complete signal gate matrix.

Just below the prime signal gate matrix, there is a sub-commutated signal gate matrix. These matrices are almost identical in detail, but the sub-commutation principle has been included because of the general feature of all the satellites; namely, that in a data frame there are prime words -- words that appear once in one data frame. The sub-commutated signals, however, do not appear once every frame, but once in a specific number of frames. For example, there may be ten signals fed into the sub-commutator matrix, and each time the main frame cycles once, one of the prime commutator positions will be assigned to the sub-commutator matrix and it will provide one of its ten signals. Thus, in ten frames each of the data words fed into the sub-commutator matrix will be passed on to the telemetry transmitter. In this respect the entire sub-commutator signal gate matrix, the decoding matrix, and a counter are identical; with the prime multiplexing and gating here included to show that quite often in these satellites there are both prime- and sub-commutators. The prime commutator serves

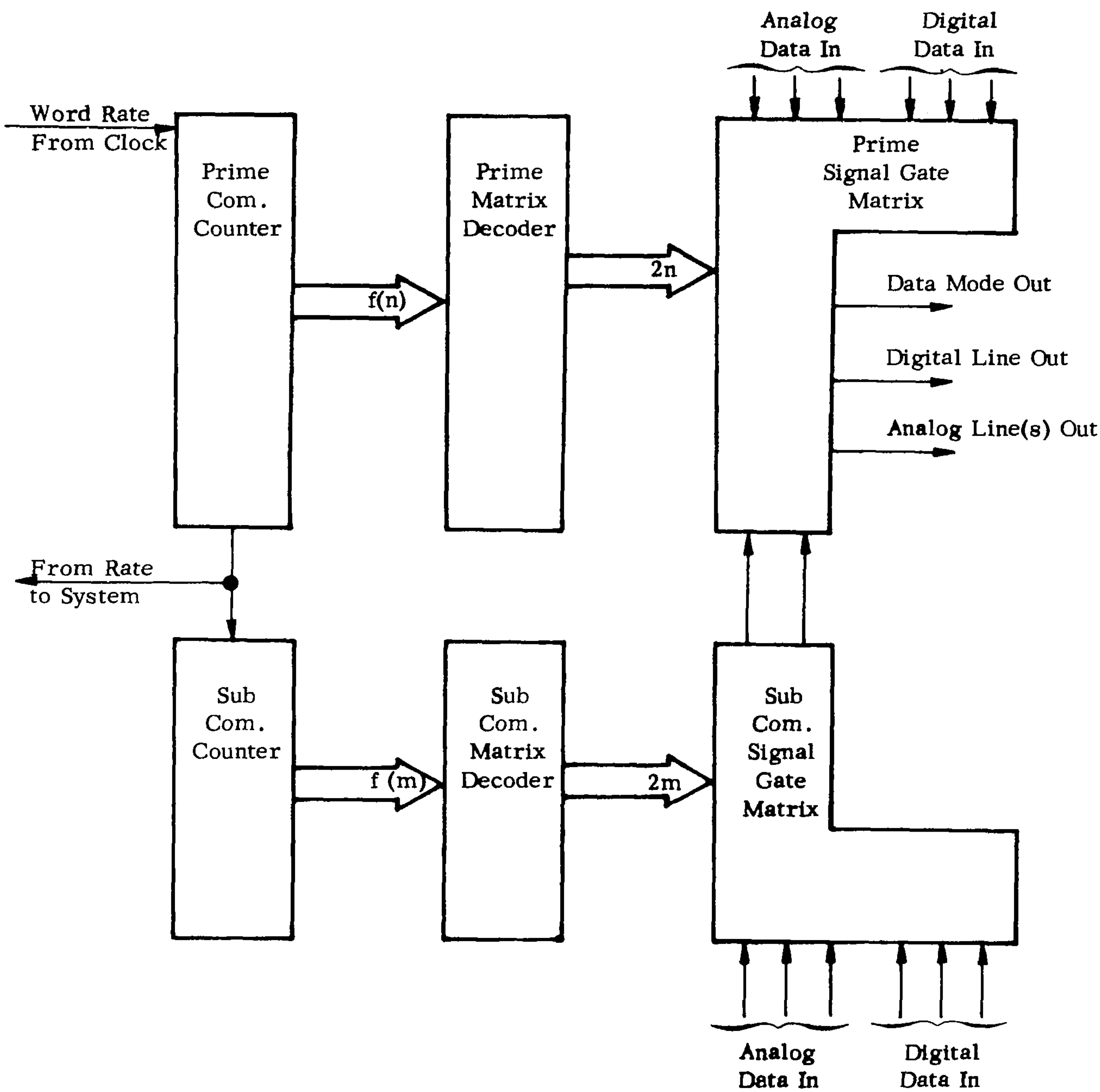

FIGURE 4.3 TYPICAL MULTIPLEXER

to illustrate the entire function of the multiplexer with the qualification that the sub-commutator is essentially constant and drives one or more of the prime signal gates.

The prime-commutator counter contains within it a count or number which determines which of the prime signal gates will be open at any given time. The word rate comes into the prime-commutator counter from a clock; and at the beginning of each word, one of the prime signal gates is closed and remains closed for the duration of the word. At the next word another gate is opened, and so forth, in sequence. The prime-commutator counter can be a simple binary counter or scaler; it also appears in several of the spacecraft in the form of a ring counter, and various other counting schemes can be arranged.

Since the powers of two are a convenient set of numbers with which to run logic, they have been chosen here to provide specific numbers to illustrate this typical multiplexer. Thus, the output of the prime-commutator counter is a function of n binary bits, the prime signal gate matrix is driven from 2^n lines, and there are 2^n gates in the prime signal gate matrix. The prime-commutator counter provides an output at the end of each frame. This occurs at the frame frequency and is distributed to the system wherever it may be required for synchronization, and in addition it is sent to the sub-commutator counter so as to sequentially close the gates in the sub-commutator signal gate matrix.

Connecting the counter proper and the signal gates is what we have called the matrix decoder. This takes the function of n bits which comes from the prime counter; and in response to each function, i.e., the 2^n binary numbers, activates a position in the decoder. For each of these numbers as it appears in the counter, one of the output lines of the prime matrix decoder is activated, which in turn drives the signal gate. Such a matrix is of more general interest since it appears as a sub-system, not only in the multiplexer, but also in the command decoder. Such a matrix decoder could then be used either in the multiplexer or the command decoder system. Diagrams of three possible matrix systems for performing this function are here presented to aid in their comparison and analysis.

System A, shown in Figure 4 - 4, consists of a four-stage logic sequence in which the signal lines pass to four blocks of transmission gates; in each block one gate is closed. Then four additional transmission gates select one of the four signals gated into the blocks as the final output.

System B, shown in Figure 4 - 5, on the other hand, is a 4 x 4 x 4 matrix driven by a ring counter. This ring counter is broken into three groups; one signal from each group activates a line in the

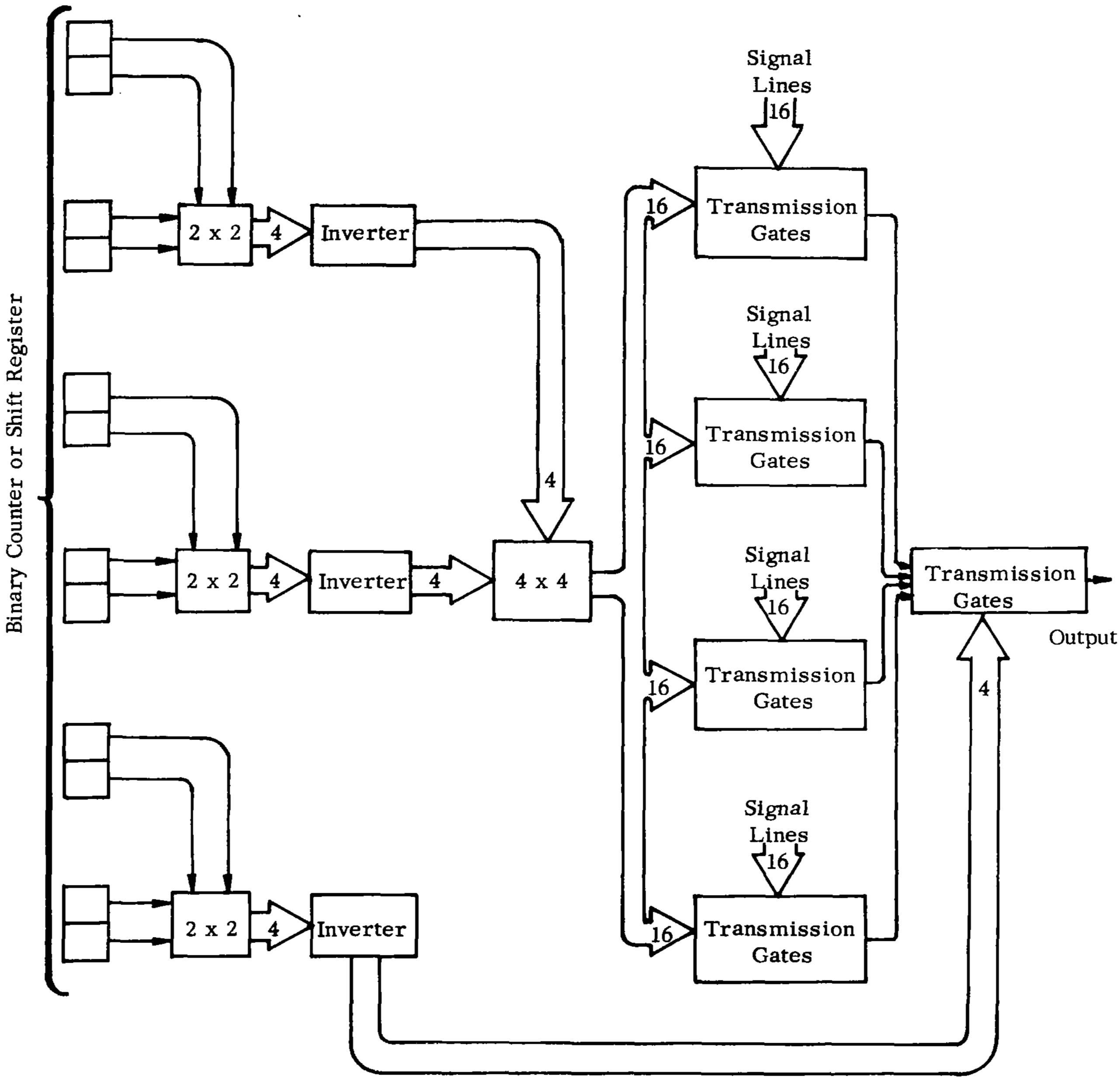

FIGURE 4.4 MULTIPLEXER - SYSTEM A

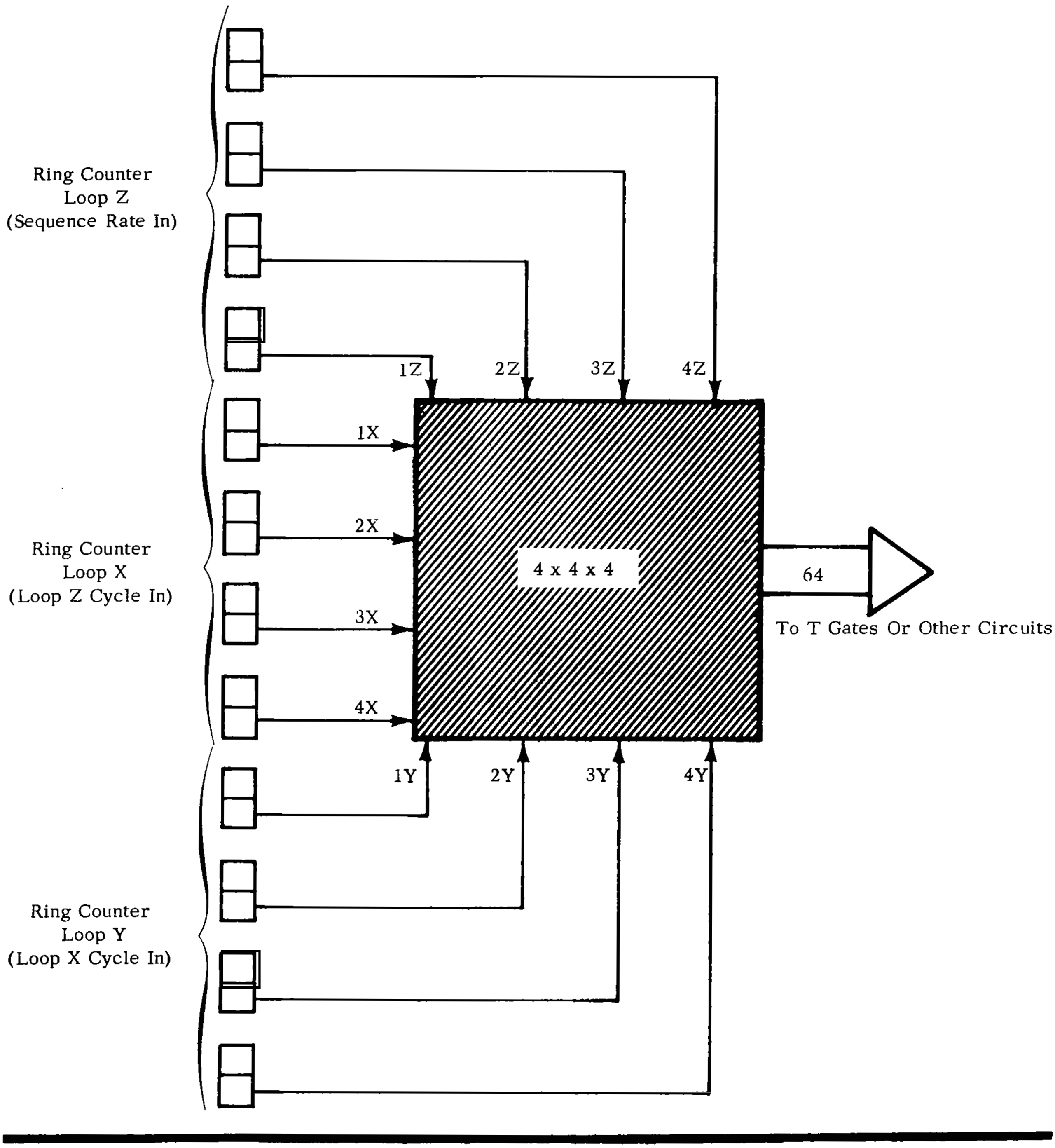

FIGURE 4.5 MULTIPLEXER - SYSTEM B

matrix, and the three signals together control one final output line by coincidence of the 3-input gates at the matrix elements.

System C shown in Figure 4 - 6 is a six-dimensional matrix in which each one of six binaries or flip-flops drives one of the input dimensions. There are sixty-four 6-input output gates; each gate is connected either to the 0 or 1 of one input dimension so as to be energized by its appropriate address only. The net result is the same as in the previous two systems.

Table 4 - 3 shows the various features of these three systems. System A is quite typical of those now used in the multiplexer of many of these satellite systems. System B is a modification allowing the use of existing microcircuitry, and is somewhat typical of those suggested for the multiplexer and to even better advantage of the command decoder.

System C, although it has some interest, is not typical for the present spacecraft circuits, since with conventional discrete components it is quite cumbersome. However, it has certain advantages and it is quite easily implemented with existing microcircuits. Sixty-four (a power of 2) has been chosen as the number of outputs and, although not universal, is a typical and useful number for this type of decoder. There also exists the possibility of cascading the decoder so that two or more could be combined to yield multiples of 64.

A number of the characteristics of the three systems have been listed in this table for ready comparison, and most of them are readily visualized. Probably the most interesting numbers are the number of modules per output. System A has less than one module per output, System B has less than 3/4 of a module per output, and System C has approximately 1½ modules per output. As to the flexibility of these three systems, System A is the least flexible, System B is moderately flexible, and System C seems to be very flexible.

On System A there are some numbers in parentheses. All three of these systems use existing microcircuitry; however, these numbers in parentheses are for microcircuit modules which do not exist but should be readily manufacturable. For example, some transistor gates are needed here which are identical with existing gates but made with PNP transistors rather than the present NPN. The scheme here is to use these PNP gates to invert the logic at every step. System A uses three stages of logic with inverters at every stage; some of the inverters are implicit in the transmission gates. If the logic were inverted at every stage instead of inverting the signals per se, one would obtain a considerable saving in the number of modules required. The numbers in parentheses indicate what numbers might be obtained if the PNP type modules existed as well as the NPN type, namely about one-third of those from a single polarity (NPN) system.

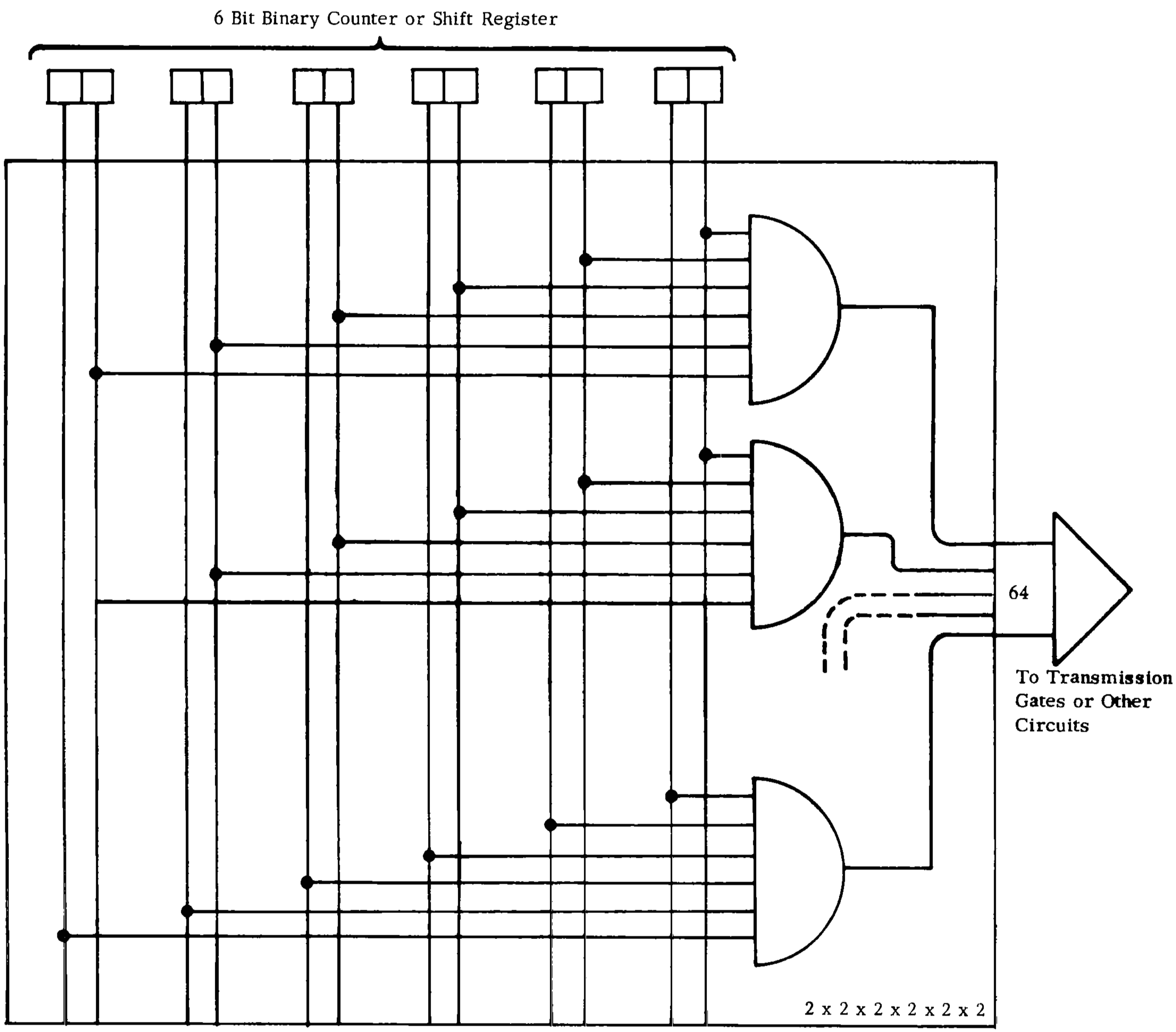

FIGURE 4.6 MULTIPLEXER - SYSTEM C

TABLE 4 - 3

MATRIX COMPARISONS

	System A	System B	System C
Number of bits	6	6	6
Number of outputs	64	64	64
Type of matrix driver	Binary Chain	Ring Counter	Binary Chain
Shift control	Yes	No	Yes
Count control	Yes	Yes	Yes
Output use	Multiplexer	General	General
Digital gates	Blocks of 16	Mixed	Mixed
Analog gates	Blocks of 16	Mixed	Mixed
Flip-flops used	6	12	6
3-input gates used	108 (28)	64	0
6-input gates used	0	0	88
Total modules used	60 (20)	44	94
Module leads used	400 (160)	416	672
Total module leads	600 (200)	440	940
T gates required	68	0	0
T gates usable	0	64	64
Modules/output	.937 (.312)	.688	1.47
Flexibility	Low	Fair	Good

Parentheses refer to NPN-PNP combinations.

System A and B are quite typical of current discrete practice. System C capitalizes on the properties of existing microcircuits, and provides a reasonable illustration of the potentialities. A further theoretical treatment of the multiplexing problem would provide a method for determining a "best" matrix. This "best" matrix could then be built as one large block and would be useful both in the multiplexer system and in the command decoding system, but as such would be too large to be practical with present microcircuit technology.

Taking System C as an example of the existing circuitry, it is the most general, it can be driven from a binary counter or a shift register which would make it applicable both to the command decoding or the multiplexing, and its output is independent of the transmission gate so that it could drive transmission gates as needed in a multiplexer, or it could drive various command lines as needed in a command decoder. System A is the other extreme. It is not applicable to the command decoder because the transmission gates are part of the system -- in fact, they make up part of the logic -- so that System A, although it is in quite common use and has advantages over System C, is not as flexible and would not work out if it were applied to a command decoder. On the basis of these three systems -- the rather large variation in the number of modules per output, and the difference in flexibility -- it may later be worthwhile to investigate more completely the theoretical possibilities for building such a matrix and then to construct one having on the order of 64 outputs. This unit should then be very useful in a variety of places throughout the spacecraft system.

Referring again to the block diagram of the typical multiplexer, Figure 4 - 3, another portion, namely the prime-commutator counter, is also of interest. There is quite a wide application for both a binary counter and a scaler throughout the spacecraft. In addition, there are a large number of shift registers. Using a binary scaler or counter in this particular spot in the multiplexer would work out very well if the prime matrix decoder was of the type previously discussed, so that one might want a counter here. As the command decoder is generally built, it might be well to have a shift register. Figure 4 - 7 shows a somewhat modified integrated microcircuit, modified to apply this concept. By connecting the units in the manner shown on this diagram, a universal counter results, i.e., by grounding the four lines and putting a clock signal into the count line, a counter which may be set or re-set by a pulse on this line is obtained; or by setting the appropriate signals into these four lines, the unit may be made to operate as a shift register. This unit could be constructed all in one piece so that it would be applicable for either type circuit. For example, in the Syncom satellite, there was a need for a unit such as this (later not used) which performs both functions, alternately or mixed. A count can be added up in the register and shifted out simply by controlling the appropriate lines with gates. The count input from the clock can be left running in continuously if desired. As mentioned,

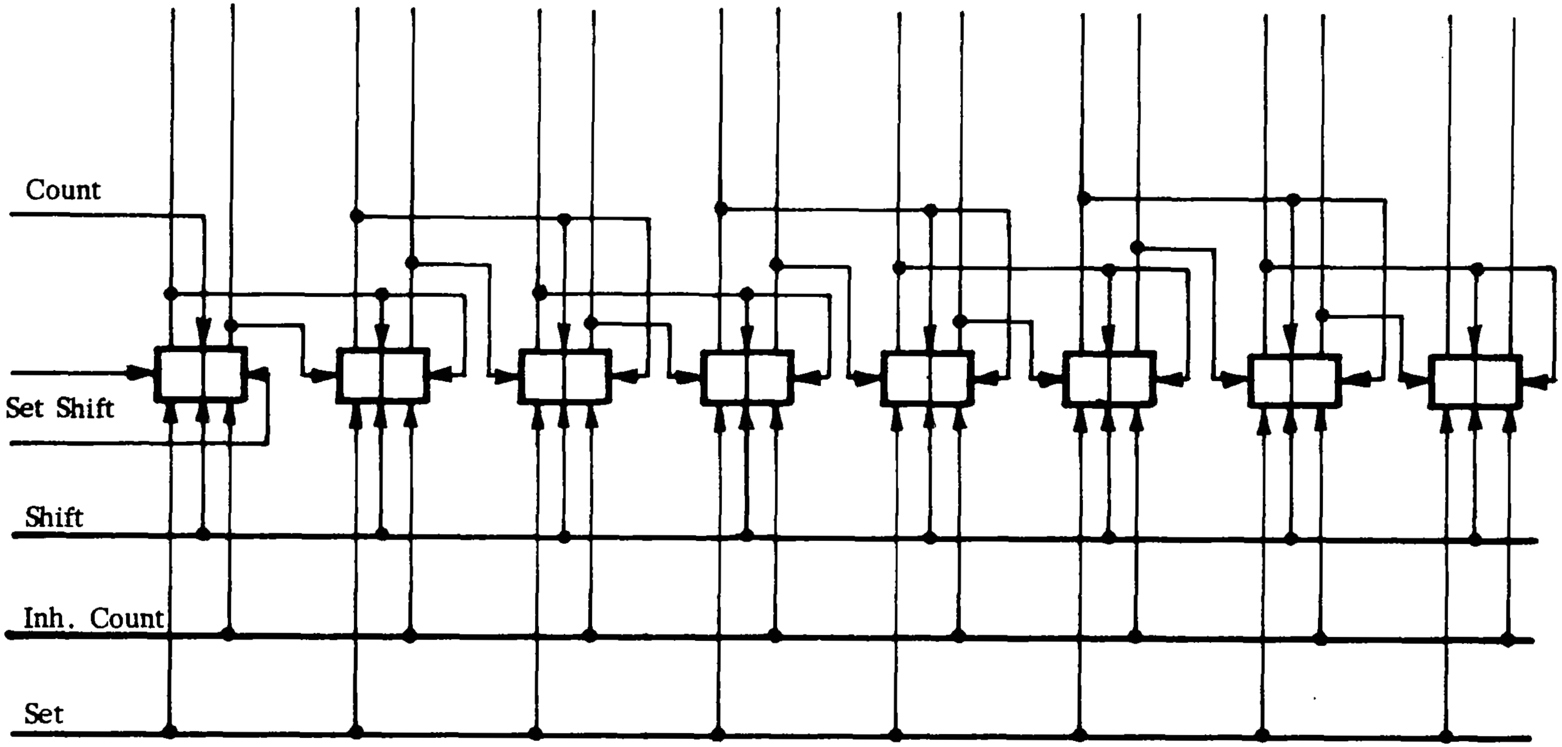

FIGURE 4.7 COMBINATION OF SHIFT-REGISTER AND COUNTER

this modified unit consists basically of the contents of a SN-511 network (Texas Instruments) with the addition of two diodes, four resistors, and two capacitors. This does not seem to be an exorbitant amount of additional circuitry to add to the basic flip-flop, and this modification could be readily made.

A number of such modified flip-flops could be welded on a small ceramic printed circuit board, permanently connected together and tested as a unit or "component". Thus, the entire sub-system could be tested to the stringent reliability specifications normally used for the evaluation of simple integrated circuits.

E. STATE-OF-THE-ART ASSESSMENT

Because technological improvements promise to further decrease the power needed for a given speed, there is a question as to when a new development program can provide devices which will be suitable for future needs. The points on Figure 4 - 1 lie relatively close to the single line drawn, indicating a constant ratio of (clock) frequency to power for simple gating circuits. However, if one compares this line with a similar one for an earlier period, one notices an improvement with time. Figure 4 - 2 shows the ratio of power to frequency for these. One can see that there has been a definite improvement since integrated circuits were first introduced. Improvements since then have been quite considerable. These have been due to the introduction of epitaxial technology, to the development of devices of much smaller size, the use of smaller structures in general, and to higher collector resistivities possible with better contact layers. These all have decreased parasitic capacitance, thus increasing circuit speed. One can expect a further gradual improvement of devices. This improvement will become quite marked when the presently developed dielectric isolation schemes for silicon integrated circuits become readily available.

In conclusion, because of the great savings in weight and volume when using integrated circuits, it would seem desirable to encourage the development of lower power devices, so as to bring the power consumption down to levels comparable with that possible using the best available discrete transistors for the speeds likely to be used by these satellites. These usually require relatively low speed devices suitable for 50 kilocycles or so. They would be adequate for most applications, and have a power consumption of 100-200 microwatts per simple gate circuit, with a flip-flop using somewhat more power. This would compare favorably with standard discrete circuits already designed for some satellites now in existence, such as IMP, which uses much low power circuitry. A further reduction in power, at low speeds, will be possible when the developments in silicon field effect transistors and metal-oxide-semiconductor (MOS) transistors result in highly developed reliable devices, both discrete and in integrated combinations.

In these discussions neither the multi-chip type "integrated" circuit nor the hybrid passive circuit with added semiconductor chips has been extensively treated. The major reason for this emphasis on monolithic silicon circuits has been their higher and partially proven degree of reliability, coupled with the fact that the higher frequency performance of these hybrids is not required in the present circuits for the applications satellites. An inspection of Table 2 - 3 suppo :s this consideration.

F. FIELD EFFECT TRANSISTORS

Although the field effect and unipolar transistors are among the earliest semiconductor devices constructed, their development has been retarded by the serious problems set by surface effects, traps, channel formation and dielectric polarization. More recently, the better understanding of these problems and the development of both depletion mode and enhancement mode field effect transistors in silicon has re-opened the question of their suitability to microelectronic or integrated circuits. Although still in the laboratory, they promise certain ultimate advantages of high impedance, switching and amplification characteristics, and very simple, direct coupled circuitry, which make them attractive for consideration in future microcircuits.

Two generic types have been developed. These are those utilizing a junction gate electrode for depletion of an existing channel, thus reducing current flow, and the insulated gate type which operates by enhancement of conductivity. The insulated gate units can, under some conditions, also operate in the depletion mode.

1. Depletion Mode Field Effect Transistors (FET)

Primarily this class of FET devices utilizes a diffused or alloyed "gate" electrode consisting of a PN junction interposed between two ohmic contacts termed "source" and "drain", which controls and constricts the intervening conducting channel. Whereas the earliest units of this type had been made by alloying, more recently diffused silicon devices utilizing the latest planar, oxide passivated epitaxial process technology have been developed. Both "P" and "N" channel devices are available with a range of electrical performance characteristics, and data on the reliability under military environments is now being obtained.

These silicon junction field effect transistors have a very high input impedance, low capacitance, and at high source impedance a very low noise figure, which is only one order of magnitude higher than the best electron tubes. Thus, they are very well suited to low power spacecraft circuits, both analog and digital. They have been used successfully in many high impedance input circuits to drive ordinary transistors and have also been used in integrated structures together with "ordinary" or bipolar transistors. Table 4 - 4 illustrates the characteristics obtainable from discrete field effect transistors, and Table 4 - 5 are those obtained in integrated devices.

While the hope has been voiced that such devices, due to their predominant majority carrier operation, would be more radiation resistant than "ordinary" transistors, this has not entirely been the case. Medium voltage units, with pinch-off voltages in the 20 to 100 volts, are somewhat better than high frequency bipolar transistors. However, FET devices

TABLE 4 - 4

DISCRETE FIELD EFFECT TRANSISTORS

Type	Silicon N Channel	Silicon P Channel	Silicon M.O.S.T.
Average Power, mw	0.1 - 50	0.1 - 40	6 - 40
Typical Operating Voltage, volts	2 - 10	2 - 8	4 - 10
Typical Operating Current, ma	0.1 - 10	0.1 - 10	3 - 8
Typical Volt Gain	10 - 50	12 - 50	20 - 120
Gain-Bandwidth Product	100 kc - 15 mc	100 kc - 5 mc	100 mc
Clock Rate	25 kc - 4 mc	25 kc - 1.5 mc	25 mc
Fanout	4	3	4
Package	Std. T.O.'s	Std. T.O.'s	Std. T.O.'s
Op. Temp. Range °C	-55 - +150	-55 - +150	n.a.
Storage Temp. Range °C	-65 - +200	-65 - +200	n.a.
Mech. Reliability - Equivalent	planar transistor	planar transistor	planar transistor
Failure Rate - Op. Life (to date)	0.5%/ 1000 hrs.	0.01%/ 100 hrs.	Not established

TABLE 4 - 5

INTEGRATED FIELD EFFECT TRANSISTORS

Type	Digital	Linear
Average Power, mw	0.1 - 20	10 - 2000
Typical Operating Voltage, volts	6	3 - 28
Typical Operating Current, ma	0.02 - 3	3 - 100
Average Typical Volt Gain	--	20
Useful Frequency Range	--	0 - 20 kc
Clock Rate	100 kc - 1 mc	--
Fanout	10	--
Package	T.O. - 5	--
Operating Temp. Range ^{o}C	-55 - +125	--
Storage Temp. Range ^{o}C	-65 - +200	-65 - +200
Mech. Reliability - Equivalent	Equivalent to S.C.I.C.	Equivalent to S.C.I.C.
Failure Rate - Op. Life	Not established	Not established

with pinch-off voltages under 10 show so much change of channel resistivity with radiation that their performance is much worse than that of low voltage, heavily doped, bipolar transistors, which are relatively insensitive to radiation.

2. Enhancement Mode Field Effect Transistors

By applying contacts to a thin layer of high resistivity semiconductor material and placing an insulated layer over the intervening region with a superposed gate contact, the insulated-gate or metal-oxide-semiconductor (MOS) field effect transistor is formed. Such devices have been made of evaporated cadmium sulfide, and more recently of high resistivity single crystal silicon. Input impedances over 10^{12} ohms are readily achieved, and transconductances of 1,000 to 10,000 micro-mhos have been reported. Some difficulties have been observed due to charges and trapping states on the oxide layer, which have led to parameter drift or variations after storage, with voltage, at elevated temperature.

As a considerable amount of effort is now being expended by the industry to overcome these parameter variations and their causes are beginning to be understood, it is expected that these limitations may soon be overcome, probably within the next two to three years. Then these devices will become extremely useful.

V. TASK 3 - COMPARISON OF MICROELECTRONIC DESIGNS BY DIRECT SUBSTITUTION

Selected subsystems in each satellite were examined in detail, to assess the possibilities of direct substitution of microelectronic elements for the discrete components. At the time of initiation of the study, no thin film or printed ceramic hybrids with attached semiconductors were readily available in sufficient volume to allow an assessment of their reliability. Thus, the direct substitution discussed in this section was restricted to semiconductor integrated circuits.

As described in the previous sections, the multiplexers, gates and digital coders and decoders are common subsystems, at least in general characteristics, to most of these spacecraft telemetry and control subsystems. Several of these subsystems could be redesigned, with only minor changes, to utilize a large fraction of microelectronic elements, namely silicon integrated circuits.

A. DIRECT REPLACEMENT OF IMP CIRCUITS BY SILICON-SUBSTRATE INTEGRATED CIRCUITS

If IMP circuits were replaced by silicon substrate integrated circuits of equivalent function, two changes would occur. First, there would be a change in the weight of the circuitry; secondly, there would be a change in the power supply requirements, as shown in Table 5 - 1. The change in power requirements can also be related to the system weight, using the weight equivalent of this power in the power supply system. Thus, the net effect of direct replacement can be expressed as a weight change in the spacecraft. Also assessed is the change in the number of connections to be made in fabricating and installing the circuits.

The effect of a direct replacement of typical integrated circuits is shown in Tables 5 - 1 and 5 - 2. The flip-flops were selected as being a typical circuit and one for which there is a readily available silicon substrate equivalent. There are primarily two types of flip-flops in IMP, both occurring in blocks of three. There are some operating at 500 KC, shown in the first column of Table 5 - 1, but most of them operate at 100 KC because speed is not needed here and they use somewhat less power, as shown in the second column. The net weight of the circuitry is listed here, which is the weight of the components and the related area of circuit board which pertains to them. The IMP flip-flop weights were computed on the basis of .35 grams per transistor, .2 grams per resistor or capacitor, .16 grams per diode and 4 grams for the circuit board (approximately 1.5 square inches). The weight given for integrated circuits, such as an SN-511, is for three flip-flops with circuit board. The weights have also been adjusted or "corrected" allowing for the allocation of weight for the proportional part of the structure, obtained by multiplying by 1.387. The net power used by the 500 KC flip-flops is just under 6 milliwatts, that used by the 100 KC flip-flops just over 3 milliwatts. To obtain gross power, one must allow for the inefficiencies of the individual converters and the inefficiency of the prime converter. This gross power, the 17 milliwatts in one case of the 9.75 milliwatts in the other case can also be converted to an equivalent weight using the weight equivalent of power, thus 11.9 or 6.8 grams leading to a total weight. This total weight represents the weight of the circuitry, plus the supporting circuit board, the proportionate weight of the power supply required for it, the supporting structure allowable to this amount of circuitry, and the supporting structure allowable to this portion of the power supply. Thus, the net weight of the electronics is reflected back to the total system weight of the satellite.

In a similar manner the silicon substrate integrated circuit, the weight of which is quite low, is increased by its proportionate

TABLE 5 - 1

WEIGHT-POWER COMPARISON OF IMP FLIP-FLOPS (BLOCK OF 3) WITH

TI SN 511

	Flip-Flop					
	IMP	500 kc	IMP	100 kc	SN	511
Net Weight, gms	23		18.5		1.5	
Corrected Weight, gms		31.9		25.7		2.1
Net Power, mw	5.88		3.36		13.5	
Gross Power, mw	17.1		9.75		39.2	
Weight Equivalent of Power, gms		11.9		6.8		27.2
TOTAL, gms		43.8		32.5		29.3
Weight Saved with SN 511, gms		14.5		3.2		
Weight Saved, Percent		33%		10%		
Leads	190		150		27	

share of other weights. The integrated circuit, with three flip-flops, only weighs 1.5 grams or "corrected" 2.1 grams. But the silicon substrate circuit as readily available used considerably more power, more than twice as much as the low-power discrete circuitry, so that when this is converted to the equivalent weight of power, one finds that the sizable total is almost as large as the weight of the three discrete flip-flop circuits. Nevertheless, there is a small weight saving. In the case of the 500 KC flip-flops, the saving by going to silicon substrate is of 33%; and in the case of the 100 KC flip-flops, the saving is about 10%. These numbers, 33% and 10%, are only significant in terms of the approximations which have been made. The power requirements of the silicon substrate circuits were estimated for operation at the 4.2 volt operating level, since catalogs list the power for operation at 3 volts and 6 volts. Furthermore, the 500 KC flip-flops in the IMP circuitry have a diode input pulse shaper. The silicon substrate circuits do not, so that if it were necessary to supply such input circuits for pulse shaping the saving of 33% would be reduced. What is significant here is that in making the comparison by direct substitution one must consider the changes in weights and in power as well as their possible compensation, so that one can make the total comparison. More significant power, and also weight savings in the power supply, would be obtained by using slow-speed integrated circuits not yet readily available, developed for very low power consumption as discussed in Section IV.

Another item of interest is the total number of leads for the components involved, as this involves the connection reliability and the possible leaks on the hermetic seals of the components. In the case of the discrete components, there are three leads for each transistor, and two for each diode, resistor or capacitor, adding up to totals of 190 and 150 leads for the two kinds of flip-flops. The silicon substrate circuitry has only nine leads on each package, for three flip-flop packages, therefore, 27 leads. Not all of these are used so that the total would be less than 27 for interconnection. The significance of this number is not only the saving in fabrication and assembly costs, but even more the improvement in reliability.

The same kind of comparison has been made on a larger scale, and Table 5 - 2 shows the weight-power comparison with direct substitution of integrated circuits into a larger unit, the digital data processor "B". This is quite typical of the circuitry used in the telemetry subsystems. Here a certain amount of weight is directly replaceable by silicon substrate circuits. One must make some approximation, since there is only an incomplete line of circuits available to perform all the functions desired. However, it can be assumed that circuits could be made in the same family and with similar switching speed, and also the same weight and power, as the Texas Instruments 51 series and other equivalent low power circuits.

TABLE 5 - 2

WEIGHT-POWER COMPARISON OF IMP DDP-B WITH SN51 SERIES

		IMP DDP-B		SN51 Series	
Weight-Replaceable,	gms	460		36	
Other,	gms	80		80	
Total,	gms	540		116	
Corrected,	gms		748		161
Net Power,	mw	96		342	
Gross Power,	mw	279		982	
Weight Equivalent of Power,	gms		193		680
TOTAL	gms		941		841
Weight Saved,	gms				100
Weight Saved,	%				11%
Leads		2800		800	

A certain amount of circuitry and weight is not replaceable, for example, connectors, magnetic cores, transformers and the like, so that there are 460 grams replaceable by silicon substrate circuitry of only 36 grams, and some 80 grams that are not replaceable. Again, these weights are corrected to include the weight reflected back to the whole satellite. Here also as in Table 5 - 1 the silicon substrate circuits compared require considerably more power than the very low power discrete circuitry now used in IMP. Thus, the total weight of 941 grams for the IMP circuitry may be compared with 841 grams obtained with direct replacements. This saving of 100 grams, or 11%, again is not particularly significant due to the approximations made. There is also a very large saving in the number of leads and connections.

B. SYNCOM

The block diagram of the Syncom telemetry and command subsystems has been illustrated in Figure 3 - 2 and discussed in general terms.

From an analysis of sections of these subsystems, 50% of the command subsystem can be directly replaced by microcircuits, with only very minor electrical redesign. The weights, volumes and other data developed for representative microcircuits (Table 4 - 2) were then used, together with half the corresponding values for the command subsystem, Table 3 - 4. A more detailed analysis was then made of the actual circuits to establish the number and types of microelectronic components, primarily integrated circuits, for this subsystem. This is summarized in Table 5 - 3, both for the half which can be completely replaced by microcircuits on line 3 and the totals, for the subsystem and on a per command basis. This subsystem has a capacity of 64 commands.

The power is approximately the same, since the initial Syncom design did not go to such extremes as far as low power switching transistors as the IMP spacecraft previously discussed. Further power savings are quite possible, either through low power discrete or integrated circuits, using integrated circuits yet to be developed or the latest discrete transistors. Very noticeable also in a comparison with the present design is the substantial reduction in external and component connections, which alone reduce to 60% with the attendant increase of wiring reliability expected from this.

The possibility of separately developing an 8 x 8 matrix decoder, with a separate shift-register to drive it, or an integral one, was also considered. This led to the analysis described in Section IV. D. (Multiplexer). From this, it appears that several alternative circuits would be suitable as command decoders, their suitability depending upon the detailed requirements envisaged for future Syncom satellites.

An interesting development in Syncom is the 6-stage counter-shift register. This could be achieved also with integrated circuits, requiring the design of new types although these could be readily adapted from present flip-flop designs, as discussed in Section IV. D. However, it should be recognized that the improvement in redundancy available through this dual design is offset by its slightly greater complexity and its non-standard integrated circuit construction. Using standard microcircuits a more useful approach would be the construction of two separate registers, one a shift-register and the other a digit counter.

The analysis of further portions of Syncom II, such as the telemetry, was pursued along similar lines; again, about half of the

TABLE 5 - 3

SYNCOM COMMAND

Example

	Volume In^3	Wgt. Lbs.	External and Component Connections	Power	MW
Present	280	1.7	400 + 2572 (2972)	1.3 standby	3.5 operation
Per/Command	4.4	.027	46	20	50
50% μ-circuits	1.18	.057	264	77.5	
Per/Command	.018	.0009	4.1	1.2	
Total	141.9	.97	1750		
Per/Command	2.2	.014	27.2		

circuits could be readily replaced by available integrated circuits with a resulting 40% reduction, approximately, of weight and volume at about the same power drain. Further replacement of discrete circuits by integrated microcircuits would require the development of new types, such as, for example, analog gates. This would lead to still greater reduction in connections and component count, as well as weight and volume. Reliability of components would be better only after these new, to be developed, components were thoroughly proven. Lower power consumption may be achieved by a redesign using either discrete or integrated components.

C. NIMBUS

A portion of NIMBUS examined specifically for conversion to microcircuits is the multiplexer. This uses magnetic cores for logic, memory and as transformers for the various gating functions. Table 5 - 4 shows the count of components. This illustration shows the much lower weight, but higher power dissipation of the integrated circuits. In fact, with a power supply total equivalent of 1.5 lbs./watt, the 15 watts higher power would require an equivalent power supply weight of 11 Kg, and thus would only be worthwhile for replacing a very heavy core matrix.

However, a redesign of this multiplexer would use fewer integrated circuits than the number postulated on an exact substitution basis. The magnetic elements are toroids of a square hysteresis loop material with several windings. Each core is "set" by driving the "set" winding with a given polarity voltage until the core is saturated. The core is reset by reversing the polarity of voltage on the same or a similarly polarized winding until the core saturates in the reverse direction. The set or reset saturation state is maintained, due to the rectangular hysteresis loop, without consuming standby energy. Thus, a core may be set or reset with only a modest energy input and remain switched without further consumption of power. This results in a considerable saving of power in a slow-speed system such as this where the switched interval is much longer than the time of transition between states.

Another advantage of this system is that it can readily commutate analog signals without materially affecting their magnitude. The control, driving, and isolation means here are combined in the one element, the switching core with its windings.

Thus, in regard to complexity and power consumption this core matrix system has excellent characteristics. It appears, however, that due to the size of the magnetic components and their associated discrete components significant reductions in the over-all size and weight of the matrix may be obtained through the use of integrated circuitry utilizing more conventional transistorized logic. The possibility of more miniaturized magnetic circuitry is not ruled out; however, suitable miniature magnetic circuits with multi-turn windings to achieve the required high impedances are not readily available.

The direct analog of the magnetic circuit functions is obtained with presently available integrated circuits, using a flip-flop to simulate the bistable core. Shift register A of Unit A was selected as an example of this substitution. This commutates four inputs to one output in response to sequencing signals. A set signal is introduced into the first input of a 4-bit magnetic shift register and shifted through at the word rate. In this manner a single core is reset at the beginning

TABLE 5 - 4

MICROELECTRONIC EQUIVALENTS FOR NIMBUS MULTIPLEXER:

(Matrix A and B, Registers A Through F)

On direct substitution:

Total number of integrated circuits	1760
Power consumption, watts	15.7
Volume, cu. in.	14.3
Weight, grams	264

Core logic multiplexer:

Power required, watts	0.5

of a shift pulse and while resetting closes an isolated transistor switch connecting one of the four inputs to the common output line.

As a given core is reset, a charge is transferred to a capacitor associated with it. In response to an advance pulse which occurs between shift pulses, this charge is used to set the following core. This action may be simulated by use of two flip-flops, each flip-flop being contained in a single integrated circuit.

The set, shift and advance signals required by the integrated register are opposite in polarity to those required by the magnetic register. This presents little problem since both polarities of these signals are available. In addition, assuming the entire multiplexer to be integrated, the pulses common to all registers can be generated at one point and fed out in parallel rather than having a discrete set of drivers for each register as is done in the magnetic system.

Failure rates of .05% per 1000 hours at elevated temperatures are now possible with integrated circuits. Extrapolating linearly to 10^6 hours yields for 16 integrated circuits 8 failures per million hour operation.

A calculation for the individual components of the magnetic 4-bit shift register based on failure rates from the "Third Reliability Assessment for OGO Yields" as shown in Table 5 - 5.

On the basis of these extrapolated figures the reliability of the magnetic and integrated systems would appear comparable. Further development will shortly bring the integrated circuits to rates one order of magnitude better than those achievable with transformers. The transistor and diode reliability will also be improved over those quoted. Nevertheless, on balance the integrated circuit registers will have a substantially better reliability.

TABLE 5 - 5

RELIABILITY ESTIMATE FOR DISCRETE CIRCUIT PARTS IN CORE MATRIX REGISTER "A"

Components	Unit Failure/10^6 hrs.	Total/10^6 hrs.
13 Transistors	.3	3.9
19 Diodes	.15	2.85
5 Tantalum Capacitors	.08	.4
4 Ceramic Capacitors	.01	.04
25 Composition Resistors	.01	.25
4 Transformers	.25	1.0
	Total extrapolated failure rate	8.44

Note: Data from "Third Reliability Assessment for OGO".

D. MICROCIRCUITS IN THE ORBITING OBSERVATORIES - AOSO

Although the subsystem layout and the number used in the three observatory platforms, OGO, OAO and OSO, differ considerably, the basic functions and complexity of the telemetry and command subsystems of these three families of spacecraft are quite closely related. A very complete redesign of the communication and data handling subsystems of the Advanced Orbiting Solar Observatory (S-67) had already been planned and preliminary results of this were available from the contractor (Texas Instruments) for this project. Making use of this information on the module counts needed to implement AOSO using either conventional or integrated circuits and the power, weight, and volume requirements of each, one can see some of the advantages to be gained by integrated circuits. Referring to Table 5 - 6 which compares the conventional circuit approach with the integrated circuit approach for AOSO, it is seen that the total module count in each case is approximately 1100. Making the indicated assumptions concerning the number of components per module in discrete circuitry, it follows that approximately 15,000 individual pieces or components must be handled and assembled to build this subsystem using conventional components. On the other hand, only 1,000 individual pieces must be handled or processed to assemble the same system using integrated circuits. From these totals it is apparent that approximately 33,000 internal connections must be made if one uses the conventional component approach while only 10,000 internal connections must be made for the integrated circuit approach. One can also estimate the number of external connections to printed circuit boards. By assuming six circuits per board in the discrete approach and 18 circuits per board in the integrated approach, approximately 4,000 external connections to the boards will be needed for the discrete design while only 1,500 are needed when using integrated circuits. This covers those portions of the discrete circuits completely replaceable by integrated circuits. The only assumption made here is that integrated gate circuits will also be available, which still have to be developed. The total number of connections, therefore, for the conventional approach is thus approximately 37,000 in contrast with 11,500 for the integrated circuits approach -- a net difference of roughly 25,000 connections. This comparison has validity for an estimate of reliability, since the figures which have been determined for integrated circuit modules already take account of any problems due to their internal connections.

One might also look at the total number of different components that must be handled for the two approaches. For the discrete component approach, it is estimated that approximately 14 different types of components will be required while only 4 or 5 different types of components are needed for the integrated circuit approach. Finally, one can compare the total weight, volume and power estimated by Texas Instruments for the integrated circuits approach versus the discrete circuit approach.

TABLE 5 - 6

COMPARISON OF CONVENTIONAL VS. INTEGRATED CIRCUITS FOR AOSO

	CONVENTIONAL				INTEGRATED			
	Flip-Flop R,S,C	Dual 2-input NAND	8-input NAND	Dual 2-input NOR	SN 510/11	SN 512/13	SN 514	SN 515
Total Module Count	474	486	131	36	474	144	466	9
No. Components/Module	18	10	10	10	1	1	1	1
Total Component Count			15,000			1,000		
Total Internal Connections			33,000			10,000		
No. Different Components			15			4-5		
Assumed No. Ckts/Board			6			18		
Total External Connections			4,000			1,500		
Total Volume (in^3)*			2,160			780 (-64%)		
Total Weight (pounds)*			65			25 (-62%)		
Total Power (watts)*			21			19 (-10%)		
Percent Wt. Saving/ 1000# Satellite			--			4%		

*Excludes tape recorders, transmitters, receivers and other analog functions.

It is seen that the total weight for this part of the system has been reduced from 65 pounds to 25 pounds -- a net saving of approximately 60%. The volume has been reduced from 2160 cubic inches to 780 cubic inches -- a net saving of 64%. The power required is approximately 20 watts in both cases. It can also be seen that the weight saving of 40 pounds is a 4% saving in the total weight of the satellite. It is expected that corresponding savings can be achieved with OGO and OAO and other satellite systems.

The other portions of the telemetry subsystem, which are not directly amenable to direct substitution of integrated circuits, are memories, tape recorders, the receivers and transmitters. In some of these cases thin-film hybrids would ideally be suitable. In practice, however, the state of the art of highly reliable circuits custom-built by these methods has not yet advanced to the stage where adequate reliability, equivalent to discrete component modules, can be expected in the next one or two years. Also, the data storage density of integrated circuit flip-flops, in spite of their small size, is not sufficient to compete on this account with any of the various magnetic or tape memories.

Thus, the portion of the telemetry and command system which is directly converted to microelectronics by means of integrated circuits, even when counting the circuit boards, has a weight and volume of only 25-28% of the discrete equipment, Table 5 - 7, and this is almost entirely accounted for by the remaining conventional circuitry.

When including the command program and experiment bit memories and clock timer oscillators, the weight and volume are 36-38% of those of the discrete design, Table 5 - 6. Finally, when the entire subsystem is compared, including tone decoder, tape recorder, transmitter, receiver, signal conditioner and cable harness, the total weight and volume of the microelectronic design are 69-71% of the original discrete circuit values.

These figures can be used for initial estimates of the improvement possible with other microelectronic spacecraft systems having a stated content of non-convertible circuits.

TABLE 5 - 7

SUMMARY - MICROELECTRONIC AOSO DESIGN

FOR TELEMETRY AND COMMAND

Convertible Electronics*	Initial Discrete Components	Redesign Integrated Circuits	 Remaining Con-ventional	Total	% Im-provement
Weight, Kg	26	0.8	5.7	6.5	75%
Volume, cu. in.	1912	196	328	524	73%
Power, watts	13.3	10	1.2	11.2	16%
Reliability, one year	83%	(with added re-dundancy)		95%	12%
Total Subsystem					
Weight, Kg	58			40	31%
Volume, cu. in.	4687			3308	29%
Power, watts	72			70	3%
Reliability, one year	81%	(with added re-dundancy)		93%	12%

*Excludes memory and clock oscillator compared to Table 5 - 6.

Abstracted from "Development of AOSA (S-67), Communications and Data Handling Subsystem", Texas Instruments, Inc.

E. COMMON SUBSYSTEMS

Table 3 - 6 listed those common subsystems deemed suitable for standardization and use with several of the unmanned spacecraft systems. From the superficial similarity of the requirements for telemetry of most of the data on satellite performance and other non-experiment data, a universal command and telemetry system could ideally be put together which could serve as back-up for the more complex switching which the larger spacecraft require for their elaborate experiments.

Such standardization of subsystems is rarely accepted by project engineers unless several performance and reliability factors are substantially better, or weight, power and size less, than is achievable with a specialized design specifically developed for each project. On the other hand, the formats required for the transmittal of telemetered data as well as command information are both partially standardized and also constrained by the use of common ground antennas, receivers and transmitters, main frequency and subcarrier allocations, and so on. Data rates are again in the same order of magnitude, so that a number of standardized subsystems, sufficiently small to fit into any reasonable spacecraft geometry, would be of advantage. These could be built, several at a time, and tested for reliability. Table 5 - 8 lists such functional assemblies which could be standardized portions of such spacecraft subsystems. These would then be combined, the programmers or separately built selectros and combiners wired for the particular program and selection sequence desired, and as many redundant similar assemblies used as is desired.

Not all of these functional assemblies, although appearing to be common to all spacecraft by functional definition, would be suitable for each type of satellite. Nor would all be suitable for a redesign with microelectronic techniques. Only the low speed, digital portions, and certain pre-amplifiers, gates and shift-registers are suitable as discussed previously.

A few other assemblies, such as a tape recorder and an analog-to-digital (A/D) converter, can be substantially reduced in weight and size through microelectronic design of the amplifying and digital switching portions of the circuit. The precision feedback resistor network, however, and electromechanical components are not yet amenable to replacement. Although thin-film resistor networks are, in principle, capable of sufficient accuracy (0.1%) for a 7 or 8 bit A/D converter, in practice the use of highly reliable precision resistors is indicated for use in the next one or two years. Thereafter, sufficient progress in thin-film multiple resistors would make fully integrated structures usable.

Thus, certain functional assemblies may be built, or redesigned, using microelectronic and integrated circuit designs, which have a

TABLE 5 - 8

POSSIBLE SPACECRAFT FUNCTIONAL ASSEMBLIES

A. COMMAND SUBSYSTEM

Receiver (136-137 MC)

* Digital Decoder (64 to 256 channels)

Tone Decoder

* Distribution Gates

Command Memory

* Shift-Register

* Combiner with Logic

B. BEACON SUBSYSTEM

Transmitter (136-137 MC)

Selector/Modulator

C. CLOCK SUBSYSTEM

Master Oscillator

** Countdown for NASA Time

** Countdown and Programmer

D. TELEMETRY SUBSYSTEM

Transmitter (136-137 MC)

* Selector and Logic

* Multiplexers: (1) Large (256, 512)
(2) Small (64,128)
(3) Subcommutator (16)

** Analog-to-Digital Converter, 7-bit

* Linear Pre-amplifier

Digital Memory

Tape Recorder (small)

---

*Adapted to design with integrated circuit

**Only partial microelectronic redesign at present sufficiently small size and weight so as to be readily adapted to any of the current spacecraft under consideration in this project. The concept of an "erector-set" satellite is, therefore, close at hand. Although additional circuits must be tailored to each system, the use of such functional assemblies with the possibility of their established reliability under severe tests makes this approach quite attractive.

VI. TASK 3 - SYSTEM CONSIDERATIONS

A. SPACECRAFT SYSTEM PERSPECTIVE

Figure 2 - 4 illustrates the development of satellite systems from the present, having three levels of organization above components, namely:

Spacecraft Electronic System

Subsystem Chassis

Modules or Cards

The improved intermediate stage is obtained by the direct substitution of microelectronic components and integrated circuits, and has two levels of organization above this integrated or microelectronic circuit:

Spacecraft Microsystem

Subsystem Modules

This underscores one major advantage, in addition to the improved circuit reliability, namely the removal (partial, at least) of the component level from the number of levels which must be tested and proven in assembling and checking out a spacecraft electronic system.

In order to be able to assess the relative importance of the improvements in reliability, power, weight, performance and other factors possible with a microelectronic redesign of certain spacecraft subsystems, the perspective of the total spacecraft system must be used in addition to the factors discussed before. Table 6 - 1 illustrates the range of weights and power allocated to various subsystems of small and medium satellites, such as Explorer, IMP, Telstar, Syncom, OSO, and others recently launched. All these use solar cell power with storage batteries and regulators, and an average weight and power range can be allocated to this power system, as well as to the mechanical structure and attitude controls.

The small satellites can be lifted into a circular orbit by the simplest booster (Scout) and into a highly elliptical orbit by an intermediate booster (Delta). The latter will also lift the medium satellites into a circular orbit, but for a very large orbit like the stationary one of Syncom, or for highly elliptical ones, a still larger

TABLE 6 - 1

SPACECRAFT WEIGHT & POWER

	Small Satellite Weight, lbs.	Medium Satellite Weight, lbs.	% of net
Typical Spacecraft gross	125-180	650-900	140%
Structure, Stabilization and Control	22-33	170-370	40%
Electronic Packages	100-150	260-640	100%
Power System	25	100-225	20-40%
Cable Harness		10-20	3-10%
Electronics & TM		100-170	20-25%
Experiments	10	140-250	33-50%

	Power, Watts	Power, Watts	% of net
Total Power (net)	20-30	175-200	100%
Experiments		70-100	40-60%
Stabilization		60-90	30-40%
Electronics & TM		15-50	10-25%
Transmitter (TM)*	1	1	1%
Net lbs./watt power system	1.15	1.15	
Gross lbs./watt power system	1.50	1.50	

*Some experiments have additional transmitters booster (Atlas) would be needed. These are compared in Table 6 - 2. From this Table one may infer the importance of keeping the weight of a satellite low, or the importance of keeping in mind a cost equivalent of a major weight reduction. However, it is not generally possible to reduce the weight of a given electronic system so far by the use of microelectronics to be able to utilize a smaller booster. This would require also a very significant reduction of power consumption and of power supply weight, not only in the electronics, but also in the experiments and controls.

Another conclusion, however, is that even a modest weight reduction may provide additional functional capability. By added electronics, at the same total weight, additional data may be obtained so as to improve the effectiveness of the spacecraft. Alternately, even a few pounds of weight reduction can double the fuel load stored in a stabilized spacecraft for attitude control and stabilization, thus doubling its life in orbit. This may be particularly applicable to Syncom, OAO, OSO, and Nimbus.

Table 6 - 1 also shows that with each direct weight saving at the spacecraft electronic system level, an additional 40% (average) saving of related structure weight, fuel for stabilization, control mechanics and so on is realized, since this 40% is the "overhead" in mechanical structure required, on a simple proportional apportionment, to hold, support and control each unit of weight. Likewise, a reduction in module size may reduce cable harnesses and supports, through a reduction in the length of all interconnections. Thus, one must consider, in weight reduction, not only the direct component weight reductions, but also the savings in related circuit board, chassis and equipment weights discussed in Section III, Table 3 - 2. In addition, the approximately 40% "overhead" for the related structure weight must be applied also. Consequently, weight savings achieved by the use of microelectronics, as seen from the systems perspective, are quite considerable.

The power system, discussed in more detail later, also requires an over-all system perspective for its total assessment. Again, the average 40% structure "overhead" applies to the weight of the power system, in converting this to total weight equivalent of power. Expressed in terms of "net" power drawn from the power system, stabilized and regulated, this becomes a weight equivalent of 1.5 lbs. per watt. Additional regulators and controls in the various subsystems are to be avoided if possible since frequently these operate at low efficiencies of 60-90%, thereby further wasting power and weight.

One possibility of lowering power consumption in the spacecraft electronics is the use, or development, of lower power digital and analog circuits, to the limits of switching speed, bandwidth and

TABLE 6 - 2

SATELLITE LAUNCH COSTS

PAYLOAD VS. BOOSTER COST

Vehicle	Stages	Payload in Pounds 345-mile Orbit	 Escape	Launch
Scout	4	150-200	--	1.0M$
Delta	3	800	120	2.5M$
Thor-Agena B	2	1,600	--	6.8M$
Atlas-Agena B	2½	5,000	750	8.3M$
Atlas-Centaur	2½	8,500	2,300	12.5M$
Saturn		20,000		17M$ project

reliability permissible. An order of magnitude, or 10 times, reduction appears possible, thus reducing the power drain of the digital portions of the spacecraft electronics to nearly negligible proportions.

About half of the electronics system can be redesigned in the manner outlined, and approximately 75% of the circuits of applicable portions of the telemetry and control system are digital, leaving 25-30% of the weight, and after development of suitable low power circuits, of the power, which cannot be reduced in this manner. Other portions of the electronic system, such as transmitters and receivers, memories, tape recorders and so on generally cannot be reduced without very drastic redesign. Thus, 65% to 70% of the system's weight and volume, and ultimately of the power drain, remains, and will have to be reduced by trade-off and redesign rather than by direct substitution of integrated circuits. This is illustrated by Tables 5 - 6 and 5 - 7 citing data on AOSO. This and the other spacecraft data presented may be summarized as shown in Table 6 - 3.

TABLE 6 - 3

WEIGHT AND VOLUME REDUCTIONS THROUGH DIRECT

SUBSTITUTION OF INTEGRATED CIRCUITS

	Approximate Reduction
Portion Completely Convertible	80-90%
Average Digital Portion Studied	65-75%
Digital Subsystem Including Memory	50-65%
Total Command and Telemetry:	
Without Recorders	40-50%
With Tape Recorders	25-35%

B. SUBSYSTEM OPTIMIZATION

The major part of this work has dealt with the immediate advantages possible with a direct substitution of microelectronic integrated circuits for discrete components. A number of these are readily apparent. However, certain disadvantages must also be considered. One of these is a certain lack of design flexibility.

Whereas out of the full spectrum of available discrete, small components there are hundreds which are suitable for spacecraft circuits of high reliability and low power, weight and size, only a few, and at best several dozen microelectronic integrated circuits, are available or will readily be built which are suitable for spacecraft with slow-speed switching. As has been shown, only one-half to three-quarters of the circuits considered can readily, and then with some degree of innovation of types, be replaced with present or to-be-developed integrated circuits. In other cases, it takes several such circuits to replace a simple discrete one.

A further negative aspect is the different logic, mostly parallel-input type, which characterizes integrated circuits and computer logic. Conversely, many spacecraft logic circuits such as those used in IMP use series connected logic or relay-tree logic, in order to provide better protection against the small probability of shorts, which is worse because of power hogging than the unreliability due to open connections.

This could be overcome by several alternatives. One could use a large series load resistor with each integrated circuit, or even operate them in series with each other across the power supply. This, however, introduces other difficulties. Another approach is to ignore this problem, except for some series resistance protection, and to count on the rather high reliability already established for present-day integrated circuits.

A further approach to the negative aspects and to the reduction of other limitations of spacecraft electronics is to use the margin of weight and size, and hopefully eventually a possible margin of power, obtained by using integrated circuits. This can be used to improve reliability by various means, such as increased redundancy or multiple performance of functions, decentralized subcommutation and switching to reduce wiring, and so on. Table 6 - 4 illustrates a number of the advantages which can be utilized, and disadvantages which must be overcome, by such a subsystem optimization.

TABLE 6 - 4

ADVANTAGES AND DISADVANTAGES OF MICROELECTRONIC INTEGRATED CIRCUITS IN SPACECRAFT

1. REMOVAL OR REDUCTION OF COMPONENT LEVEL

   a. Variety and Number of Parts
   b. Testing Simplification
   c. Reliability

2. DIRECT SUBSTITUTION

   a. Direct Savings - Weight, Size, Reliability
   b. Indirect Savings - Connections, Hermetic Seals
   c. Negative Aspects - Shorts, Lack of Flexibility

3. SUBSYSTEM TRADE-OFFS MADE POSSIBLE

   a. Minimum Parts Used Repetitively
   b. Different Logic of Subsystem Connections
   c. Reliability Through Multiple Components or Majority Logic

4. OTHER SYSTEM TRADE-OFFS

   a. Central Vs. Decentralized Switching
   b. Wiring Multi-Wire Vs. Parallel
   c. Redundancy Aspects

C. THE CONNECTION PROBLEM

1. Cables, Connectors and Wiring Harness

From Table 6 - 1 and other data, it can be seen that the cable harness represents at least 3% of the weight of a medium-sized spacecraft electronic system. When one adds to this the sockets and connectors on each subsystem chassis as well as printed circuit connectors, the total may rise to as much as 10% of spacecraft weight. Clips and mounting brackets similarly contribute to the structure by a comparable amount.

The reliability to be expected from connectors is relatively poor, being comparable to subsystem reliability rather than component reliability, as the failure rate per lead (Third OGO Reliability Assessment) is 0.2 failures per 10^6 hours or 0.02% per thousand hours. Each wire connection between two chassis goes through four connectors, resulting in a failure probability of 0.08% or almost 0.1% per thousand hours for each wire interconnection.

This provides one of the reasons why Telstar and a few other spacecraft systems have eliminated most connectors, and instead use soldered-in or welded interconnections. Even with improvements in connectors and terminals, a considerable improvement in system reliability can be obtained by a new approach to the connector problem. In addition, in a microelectronic system, the conventional connectors are so large as to occupy almost the whole front panel of the subsystem.

A solution which is beginning to be used, for example in Explorer and IMP, involves the utilization of remote subcommutation of experiment data at the data source or in the pre-amplifier chassis, so as to reduce the number of data wires leading to the central telemetry subsystem chassis. The inference from this study is that as many as ten integrated circuits with a failure rate of 0.002% per thousand hours could be added or substituted, in a revised system, for each wire lead saved with a net improvement in reliability of the order of half of that of the original total interconnection or 0.04% per thousand hours. Table 6 - 5 illustrates this with a hypothetical example. By doubling up terminals and wiring for the signal line, a considerable improvement in reliability is obtained, and in fact loss of a binary subcommutator drive line now only affects 50% of the data. Thus, a 3-6 fold or greater improvement in reliability may be achieved with a 3-fold or greater reduction in wiring. Even more striking is the application of this approach to larger groups of data lines, but it is only realistic to apply the subcommutator technique in cases where the additional power can be readily furnished. Of course, in some cases the subcommutator simply replaces the corresponding section of a central commutator, thus not requiring additional circuits in this system. But

TABLE 6 - 5

TIME DIVISION VERSUS MULTIPLE WIRE INTERCONNECTIONS

	Wires	Terminals	Flip-Flop Circuits	Failures/ 10^6 hr.
16-line conventional wiring	16	64		13
16-line subcommutator and data, sync lines (counter)	2	8	48	2.6
16-line, using parallel binary drive	5	20	16	4.3
16-line, also two signal lines	6	24	16	2.0
16-line, also added power wires	8	32	16	2.0

frequently the data lines cannot be so readily grouped, so that some circuit duplication may be required.

The weight saving from this approach is quite considerable also. At the printed circuit board level, connectors weigh about 20 grams for 8-16 pins, an incremental weight of 2 grams per pin or wire, on the supposition that there is negligible weight associated with the printed circuit male connection on the board. The larger cylindrical connectors contribute about the same or slightly more per pin, but here four connectors (both male and female at both ends of the cable harness) must be counted. The wire weight itself doubles such a weight figure again, thus each wire run contributes of the order of 20 grams net weight which would be eliminated by the reduction of wiring contemplated. In the example of Table 6 - 5 the change from 16-line conventional wiring to 8-wire partially redundant wiring with 16-unit subcommutation reduces the net weight of wiring and connectors by an average 150 grams, or a gross spacecraft weight of 200 grams (nearly ½ lb.). The added power, if required at all, is only of the order of 100 milliwatt, so that the added power system weight would also be (at 1.5 lb./watt), much less than the weight saving in wiring.

The same approach may at times be applied to wiring and connectors to the printed circuit board within a chassis. Here, however, the space and weight margin for the subcommutation may not be available, and a better approach here is to eliminate connectors entirely by permanently wiring or welding the circuit cards into place.

These sample computations illustrate the substantial weight reductions which can be accomplished by reducing connectors and harness wiring, first through the reduction of connectors, and finally by means of subcommutation techniques made more attractive by the low size and weight of microelectronics.

2. Subsystem Connections Between Functional Modules and Components

An assessment of the number of external and internal connections required may readily be made both for a discrete and a microelectronic or integrated circuit. In order to develop some general guidelines, a 3 or 4 input gate is used as the basic element. This has 8-12 components and a total of 20-25 internal connections and 7-8 external leads, depending somewhat upon the circuit configuration. Further data, abstracted from various computer diagrams, is illustrated in Tables 6 - 6 and 6 - 7. From these, one may generalize as follows:

a. The number of total connections in discrete digital circuits rises linearly with the number of components, at an average of 2.5 connections per discrete component. (A little over one connection for each component lead.)

TABLE 6 - 6

CONNECTIONS REQUIRED FOR VARIOUS MODULES

Module	Discrete Number of Components	Number of Connections	
		Total	Functional
(Transistor)	(1)	(3)	(3)
Gate	8	20	7
Flip-Flop	16	60	8
4-bit Register	64	50	9
8-bit Register	128	300	10
24-bit Arithmetic Unit	11,000	26,000	80

TABLE 6 - 7

CONNECTIONS REQUIRED FOR VARIOUS SUBSYSTEMS

Subsystem	Number of Modules (basic gate)	Number of Total
Flip-Flop	2	16
Binary Counter Bit	6	60
4-bit Up-down Counter	24	200
24-bit Arithmetic Unit	10^3	10^4

b. The number of functional (external and power) connections or leads is proportional to the cube root of the number of components, or with a different proportionality constant, to the cube root of the number of basic functional modules (gates) used in a module or subsystem.

c. The number of components per module is of the order of 8 to 10.

d. The number of functional inter-module interconnections can be quite large and can approach 10 times the number of basic modules (gates) slightly larger than the number of leads on these.

Thus, we may generalize as shown in Table 6 - 8 which compares algebraically the number of external and internal connections.

It is apparent from these tables that the number of external leads in even a small module is fairly large, due to the fact that ground and one or even several power and bias supply leads must be brought into each module containing active elements. These small modules would be used in large quantities so that it would be generally more economical for module wiring and connections to use the largest practicable module size, and thus the fewest modules.

The conclusion to be drawn for microelectronic hybrid and integrated circuits is two-fold. Firstly, only the module interconnections are wired conventionally; the "components" being on one substrate and connected together by an evaporated circuit layer. Secondly, the module is tested environmentally as a "component", and only accepted if reliable. Thus, only the module interconnections remain to be tested or estimated for reliability after subsystem assembly.

This latter fact is quite important and is often overlooked. In fact, by using ceramic (high temperature) mother-boards and assembling integrated, discrete or hybrid circuits together into fairly large modules and thoroughly testing these assembled modules to all "component-style" environmental and electrical tests, a reliable set of building blocks for spacecraft use may also be built, having only the weight penalty of the ceramic substrate.

TABLE 6 - 8

EXTERNAL AND INTERNAL CONNECTIONS SUBSYSTEM OF

N MODULES OF M COMPONENTS

Number of	Component	Module	System
Components	1	M	NM
Modules	-	1	N
External Leads (L_C, L_M)	2-3	$3M^{1/3}$	$3.6\ (MN)^{1/3}$
Same Basic Gate (N = 8)	-	6-8	$7\ (M)^{1/3}$
Discrete: Interconnections	-	2.4 M	2.4 (MN)
In terms of component leads	L_C	$1.2\ M\ L_C$	
Modular: Interconnections	-	-	$3.6\ M^{1/3}N$
In terms of module leads		L_M	$1.2\ N\ L_M$

D. POWER AND WEIGHT TRADE-OFF

For ten satellites the effect of a reduction of the electric load power level upon the weight of the power system has been analyzed. Detailed calculations for two types of duty cycle indicate that weight reduction of 0.9 to 12 lbs. can result from average load power reduction of one watt. Approximate calculations are shown to be convenient but of limited value. Figures on additional satellites, where available, have been included for comparison.

1. Introduction

The purpose of this analysis is to estimate the total savings in weight of a satellite caused by the reduction of load power by one watt due to the use of microelectronics. The analysis is symmetrical; it also gives the added weight due to an increase in load power. The satellites considered include Syncom, Nimbus, OGO (EGO and POGO-1), OAO, and IMP. Furthermore, useful information was obtained concerning the power systems of Explorer XII, Relay, Telstar, and UK-1. A limited analysis of these data was also performed for the purposes of comparison and completeness.

Table 6 - 9 summarizes the pertinent characteristics of the electric power systems for the ten satellites considered. Three types of cell mounting are encountered: panels, paddles and body mounting. Solar panels are covered on one side only with solar cells and can be oriented toward the sun. Paddles are covered on both sides with cells and cannot be oriented. Usually four paddles are used, arranged tetrahedrally. Spin stabilized satellites employ solar cells mounted symmetrically on the body of the satellite. In general, solar panels are the most efficient and body-mounted cells the least efficient configuration, as can be seen by a comparison of the figures for average watts delivered per pound of solar array. In Table 6 - 9 the value of maximum power developed by the array refers to the optimum orientation of the satellite in space at sunlit equilibrium temperature. The average power developed by the array depends upon many factors, including the nature of the orbit, the fraction of eclipse time, the degree of degradation by radiation, the temperatures of the cells and the orientation with respect to the sun. The average power, P_a, refers to the illuminated portion of the orbit only and to the beginning of the mission, before radiation degradation becomes significant. In the table, the area of the array includes only the surfaces covered by cells and not, for example, the back of solar panels. The weight of the array includes cells, covered glasses, adhesives, substrate, wiring harnesses, booms, and other structures associated with paddles or panels. On body-mounted cells, only the weight of the substrate on which the solar cells are mounted is included.

Detailed information on the storage subsystem was available for nine satellites and total weight is known for all ten. This weight

TABLE 6 - 9 — SATELLITE POWER SYSTEM CHARACTERISTIC

		POGO-1	SYNCOM II	NIMBUS B	EGO	OAO	IMP	EXPL. XII	RELAY	TELSTAR	UK-1 (ARIEL I)
PRIMARY DATA											
Array:	Cell mounting	Panels	Body	Panels	Panels	Paddles	Paddles	Paddles	Body	Body	Paddles
	Number of cells	32,500	22,420	11,000[a]	32,500	53,000	11,520	5,600	8,400	3,600	4,256
	Max. power, watts	560[b]	147	440	560[b]	772[c]	74.3	20.4	35	15	11.7
	P_a; av. power, watts	490	135	400	490	618[e]	59.5[e]	16	28[e]	13.1	9.4[e]
	Area, ft^2	78	61.7	43	78	187	28.7	15.3	17.6	15.5	11
	Weight, lb.	127	22.1	64	127	222	26.5	11.0	25.8	26	8.8
Storage:	Battery type	Ni-Cd	Ni-Cd	Ni-Cd	Ni-Cd	Ni-Cd	Ni-Cd	Ag-Cd		Ni-Cd	Ni-Cd
	Number of cells	44	96	160	44	22	11	13		19	10
	Rated cell capacity, a.h.	12	6	4.5	12	20	5	5		6	6
	Av. discharge voltage, v.	1.25	1.25	1.25	1.25	1.25	1.25	1.11		1.25	1.25
	Av. discharge current, a.	10.1	4.57	8.6	8.9	12	2.6	1		1.1[e]	0.4
	Av. charge voltage, v.	1.45	1.45[e]	1.45	1.45	1.4	1.45	1.4		1.45[e]	1.45
	Weight, lb.	74	60	113	74	177	6.8	6.3	28	11	14
Converter-regulator:	Efficiency %	90[e]	90[e]	0.9[e]	0.9[e]	0.9[c]	0.9[e]	0.9[e]	0.9[e]	0.92	0.9[e]
	Weight, lb.	16.8[e]	23.4	12.3[e]	16.8[e]	23.2[c]	2.2[e]	6.1[e]	10.5[e]	7	3.5[e]
Orbit:	Period, min.	96.5	1,440	107	2,580	101	9,600	1,590		158	100
	Max. eclipse, min.	35	69	38	120	36	30	30		30	35[e]
DERIVED PARAMETERS											
Array:	Weight per area, lb/ft^2	1.63	0.36	1.49	1.63	1.19	0.93	0.72	1.47	1.68	0.80
	Average watts/ft^2	6.3	2.19	9.3	6.3	3.3	2.1	1.05	1.59	0.85	0.85
	Average watts/lb.	3.9	6.1	6.3	3.9	2.8	2.25	1.45	1.09	0.50	1.06
Storage:	Average disch. depth, %	25	20	15	75	36	30	10		9.2	5
	P_d, average disch. power, w.	283	128	210	248	330	37	14.4		26.2	5
System:	P_1, average load, w.	300	115	214	300	312[e]	24	14	16.8[e]	7.6	5
	W_s, total system wt., lb.	218	105.5	189	218	423	37.2	23.4	64.3	44	26.3
REDUCTION IN WEIGHT	Approx.	0.73	0.80	0.89	0.73	1.36	1.55	1.67	3.83	5.8	5.25
PER LOAD WATT ELIMI-	Case 1	0.86	0.95	0.96	0.68	1.38	1.03			4.22	
NATED, lb/watt	Case 2	1.46	12.0	2.09	7.55	2.64	N.A.			7.42	

Notes for Table (Data obtained from references 1 - 8.)
a. 2 x 2 cm^2; all others 1 x 2 cm^2.
b. at 60°C; all others at sunlit equilibrium temperatures.
c. average power from cold to hot paddle.
e. estimated.

includes batteries, battery boxes, hangers and wiring harnesses. The weight of the converter-regulator is known only for Telstar and was estimated for the other satellites.

2. Analysis

a. Classification of Weight Savings

The weight savings caused by reduction of load power are principally due to weight reductions in each of the three major subsystems: the array, the storage battery, and the regulator-controller. These are the only savings included in the present analysis. Another potentially important factor, omitted for lack of data, is the concurrent reduction of the weight of the satellite structure used to support these three subsystems. This factor could be estimated by appropriate scaling.

b. Schematic of Typical Power Systems

Figure 6 - 1 shows a typical satellite power system, in which power levels are defined as follows: P_a is the average power developed by the solar array during the sunlit portion of the orbit; P_d is the average discharge power developed by the storage battery during the eclipse time; and P_1 is the average power consumed by the load during the entire orbit. A battery-charging circuit is shown as a component of the regulator-converter subsystem, and its efficiency is assumed to be 90%. The efficiency of the regulator-converter is known for Telstar and IMP and was estimated for the other satellites to be 90%, which is probably optimistic.

c. Effect of Duty Cycle

For the purpose of estimating weight savings, the load power, P_1, may be divided into two types: power derived from the storage system and power derived directly from the array. A reduction in power from the storage system would produce a considerably greater weight savings than that derived from the array, for two reasons: the necessary capacity of the battery and the inefficiency of the battery charging. The latter inefficiency may be ascribed to losses both in the charging circuit and in the battery itself.

Two aspects of the duty cycle tend to increase the necessary capacity of the battery and consequently the weight per unit power of the system. These characteristics are a large fraction of the orbit in eclipse and peak loads which are large compared to the average load power. In general, a poor match of the load power with respect to the array power, both as functions of time, increases the necessary storage capacity and the weight of the system.

d. Approximate Weight Savings

Because the details of the duty cycle are not available for all of the satellites considered, it is necessary to estimate the weight savings approximately. The simplest approximation is the ratio of total system weight, W_s, to the average power consumed by the load, P_1. This estimate is based upon three assumptions:

(1) It is possible to reduce the weight of components in a continuous fashion.

(2) The weight of the array is linear with its average power; the weight of the battery is linear with its capacity; and the weight of the regulator-converter is linear with its average power rating.

(3) The reduction of the load power by one watt reduces the capacity or intensity of each subsystem by the same factor.

The first two assumptions are believed to be good. Assumption (1) will be most accurate in cases where the power saved is a large fraction of the normal load, and assumption (2) will be better where the power saved is a small fraction, but neither is considered to be seriously inaccurate. Assumption (3) is not generally accurate due to the power mismatch previously described. Nevertheless, this simple approximation for pounds saved per watt of load power eliminated has been calculated for each of the satellites and is listed in Table 6 - 9 In order to estimate the accuracy of this approximation, we have analyzed the weight savings in more detail for seven of the satellites, for which sufficient data were readily available.

e. Details of Weight Savings

The method is illustrated for Telstar and is also applied to POGO-1, SYNCOM II, NIMBUS B, EGO, OAO, and IMP.

The known continuous demand on the Telstar array including normalized low peaks for radiation experiments and telemetry is 4.3 watts, including 10% conversion loss. Since the average array power is 13.1 watts, the power available for battery charging P_c is 8.8 watts during 128 minutes per orbit, giving an energy of 18.8 watt-hours. This energy is reduced to 15.2 wh by the two series inefficiencies of the converter-regulator and of the charging circuit. Energy available for discharge, E_d, is reduced further by the kinetic losses of the charging process:

$$E_d = \frac{E_c V_d}{V_c} = \frac{15.2(1.25)}{1.45} = 13.1 \text{ wh}$$

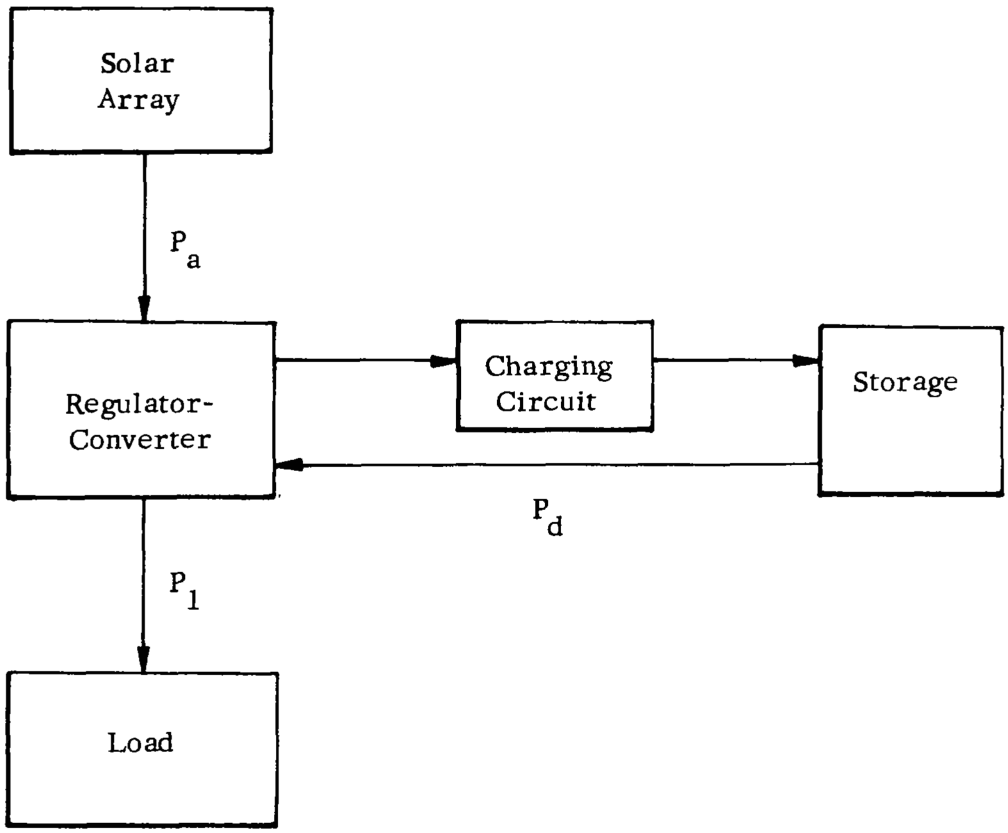

FIGURE 6.1 BLOCK DIAGRAM OF TYPICAL SOLAR POWER SYSTEM

where E_c is the energy used in charging, V_d is the average discharge voltage per cell, and V_c is the average charging voltage per cell.

For simplicity, it is assumed that all battery discharge occurs during the 30-minute (average) eclipse position of the orbit. Thus, the discharge power, P_d, is 26.2 watts. The corresponding power from the converter-regulator to the load is 23.6 watts. Of this, 3.87 watts is consumed by the continuous load, and 19.7 watts (average) is available for communication experiments. Since these experiments require 26.1 watts, they can be performed for only 23 minutes of each 30-minute eclipse. In practice, this was achieved by averaging longer and shorter periods of communication on consecutive orbits.

The savings in power system weight will be computed for two cases of interest. Case 1 is the straightforward reduction of load power by one watt continuously throughout the orbit. Case 2 is the reduction of <u>average</u> load by one watt, accomplished by eliminating 5.26 watts during the 30-minute eclipse only. The fundamental assumption for both cases is that the average depth of battery discharge is kept at its normal level, 9.2%. Thus, the capacity and weight of the battery is reduced by the fraction of discharge power eliminated:

$$\Delta W_b = \frac{\Delta P_d}{P_d} W_b \qquad (1)$$

where ΔW_b is the reduction in normal battery weight, W_b, and ΔP_d is the reduction in normal discharge power, P_d.

ΔP_d is related to the reduction $\Delta P_1'$ in load power during eclipse:

$$\Delta P_d = \frac{\Delta P_1'}{\eta} \qquad (2)$$

where η is the efficiency of the regulator-converter. Similarly, the reduction ΔW_a in array weight W_a is related to the reduction ΔP_a in array power P_a.

$$\Delta W_a = \frac{\Delta P_a}{P_a} W_a \qquad (3)$$

The reduction in array power is the sum of two terms:

$$\Delta P_a = P_c \left(\frac{\Delta P_d}{P_d}\right) + \frac{\Delta P_1''}{\eta} \qquad (4)$$

where the first term is the reduction of battery charging power and the second term is the reduction of power for the load. P_c is the power normally available for charging and $\Delta P_1''$ is the reduction of load power during the sunlit portion of the orbit.

Finally the reduction ΔW_r in the weight of the regulator-converter W_r may be approximated by the relation

$$\Delta W_r = W_r \frac{\Delta P_a}{P_a} \qquad (5)$$

Combination of Equations (1) - (5) yields the following expression for the total reduction ΔW_s in the weight of the power system, W_s.

$$\Delta W_s = \Delta W_a + \Delta W_b + \Delta W_r$$

$$\Delta W_s = \frac{1}{\eta P_d} \left[\frac{(W_a + W_r)}{P_a} (P_c \Delta P_1' + \Delta P_1'' P_d) + P'_1 W_b \right] \qquad (6)$$

For Telstar, this reduces to $\Delta W_s = 1.41 \Delta P_1' + 2.81 \Delta P_1''$

For Case 1, $\Delta P_1' = \Delta P_1'' = 1$ watt and $\Delta W_s = 4.22$ lbs.

For Case 2, $\Delta P_1' = 5.26$ watts, $\Delta P_1'' = 0$, and $\Delta W_s = 7.42$ lbs.

For simple approximations described previously,

$$\Delta W_s \approx \frac{W_s}{P_1} = 5.8 \text{ watts}$$

In the case of Telstar, the approximate value is nearly the average of the calculated values for the two cases. In the case of OAO, as shown in Table 6 - 9 , both cases give a higher weight savings than the approximate value, which indicates that caution should be used in applying simple ratios to estimates of weight reduction. However, the assumption that peak loads occur only in eclipse is pessimistic and tends to increase the disparity between Cases 1 and 2. Nevertheless, the detailed analysis, based on Equation (6) and reasonable assumptions about power load reductions during eclipse and sunlit times, is considerably more realistic than the simple ratio W_s/P_1.

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VII. CONCLUSIONS

A. GENERAL

The analysis presented in this study has shown a number of advantages of microelectronics in general and particularly of presently available silicon integrated circuits or those readily developed. In view of several problems associated with the use of hybrid and also of integrated circuits, the application of hybrid thin-film circuits to spacecraft electronics is not yet fruitful, but will be possible after sufficient data on reliability is accumulated. At present and in the near future, silicon integrated circuits of low power consumption are, on balance, advantageous for use in and redesign of unmanned spacecraft electronic systems wherever applicable. This is particularly so in the non-radio frequency portions of the telemetry and command subsystems of the spacecraft studied. This is outlined in Table 7 - 1.

Integrated circuits are available with power consumptions as low as most discrete circuits examined, although not with as low a power drain as is ever achievable with the best low-power transistors developed. Thus, there is no direct power advantage in using integrated circuits. It is to be hoped that some of the most recently developed isolation techniques will overcome this disadvantage and that such units, when developed, will be reliable.

There are substantial weight and size advantages to using integrated circuits even sufficient to balance, on a system trade-off, the additional power supply weight needed to supply the additional power drawn by an integrated circuit version of the circuits studied.

Direct substitution of circuits in the digital portions of the subsystems is a relatively straightforward procedure, requiring only a moderate redesign of most circuits. It is not the most "economical" (in weight, power, functional simplicity and reliability) solution, but minimizes the redesign and marginal testing required in conversion to microelectronics.

The radiation tolerance of silicon integrated circuits is theoretically similar to that of circuits made up with discrete components. In practice, smaller size of most integrated active devices may actually advantageously offset the much larger number of transistors used in integrated than in discrete circuit modules.

A number of apparent advantages of microelectronic circuits in spacecraft are advantages which could be obtained from other circuitry, but which can only be realized because of the small size, low weight, and fairly low power (when applicable) of integrated and

TABLE 7 - 1

SUMMARY OF BENEFITS FROM MICROELECTRONICS

Major Advantages

LOW WEIGHT AND SIZE	- Ten-fold reduction
RELIABILITY AT FUNCTIONAL BLOCK LEVEL	- Less testing needed
DIRECT SUBSTITUTION POSSIBLE	- Standard units useful
SUBSYSTEM TRADE-OFFS	- Fewer leads
SATELLITE SYSTEM TRADE-OFFS	- Reduced power possible
"OVERHEAD" TO SATELLITE PAYLOAD	- Reduced weight and size magnified

Problems

NO DIRECT POWER ADVANTAGE	- Parasitic capacitance problem
ONLY FEW PARTS PURCHASED	- Costly manufacture
PROTECTION AGAINST SHORTS	- New logic needed
LACK OF FLEXIBILITY	- Can be overcome
LOW POWER ELEMENTS NEEDED	- No commercial interest

hybrid circuits. These include the full testing of modules instead of (or in addition to) the components by the supplier to extremes of stress, permitting accelerated testing of new modules, and also include a number of system trade-offs in system design.

B. REQUIREMENTS FOR FURTHER APPLICATION

From this analysis of the telemetry and command subsystems, one can identify a number of common modules and elements, as well as other blocks or assemblies and subsystems, which could serve as further building blocks for future spacecraft electronic system design. Present integrated circuits are applicable in medium-power form primarily in the form of digital multi-input gates, flip-flops, digital buffers, differential amplifiers and choppers, practically all with NPN transistors.

Expansion of this line to include a PNP series of integrated circuits and a line of very much lower power drain, even though lower speed, elements is required for these spacecraft. These, as well as the more elaborate modules discussed in this report, are summarized in Table 7 - 2.

In order to evaluate thin-film and ceramic hybrid circuits of latest design for satellite use in the more distant future, much more reliability data will have to be accumulated, to match the information now available on the simpler integrated circuits. Insufficient data is also available to date on the radiation tolerance, in a simulated space environment, of hybrid, thin-film and even of integrated circuits. Such comparisons are only now being initiated with sufficient detail to be applicable.

TABLE 7 - 2

MICROELECTRONIC NEEDS FOR SATELLITES

Elements

1. Low Power Digital NPN and PNP
2. Pre-amplifiers
3. Low Power Transmission Gates

Blocks and Assemblies

1. Matrix 4, 8 and 16
2. Shift Register 4, 7 or 8
3. Counters
4. Parallel to Serial Converter 4, 7 or 8

Subsystems

1. Analog/Digital Converter
2. Line Concentrator or Commutator 8 and 16
3. Multiplexer 64 (8 x 8), 256 (16 x 16)
4. Command Decoder

VIII. ACKNOWLEDGEMENT

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NASA-Langley, 1965